

PIC10F220/222 Rev. A Silicon Errata

The PIC10F220/222 parts you have received conform functionally to the Device Data Sheet (DS41270B), except for the anomalies described below.

All issues listed here will be addressed in future revisions of the **PIC10F220/222 silicon**. Where noted, problems apply to listed revision only.

1. Module: Analog-to-Digital (A/D) Converter

PIC10F220/222 silicon Rev. A1. The A/D Converter does not meet the design target. The specifications listed below in Table 10-6 supersede Table 10-6 in DS41270B.

TABLE 10-6: A/D CONVERTER CHARACTERISTICS AT 8 BITS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A03	EIL	Integral Error	—	—	±2	Lsb	VDD = 5.0V 25°C
A04	EDL	Differential Error	—	—	-1 ≤ EDL ≤ 2	Lsb	VDD = 5.0V 25°C
A06	E0FF	Offset Error	—	—	±2	LSb	VDD = 5.0V 25°C
A07	E0N	Gain Error	—	—	±2	LSb	VDD = 5.0V 25°C
A10	—	Monotonicity	—	not warranted ⁽¹⁾	—	—	VSS ≤ VAIN ≤ VDD

* These parameters are characterized but not tested.

† Data in the “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only are not tested.

Note 1: This will be addressed in future silicon revisions.

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FIGURE 1: TYPICAL DNL AT 2.0V (TESTING AT 7-BIT LEVEL)

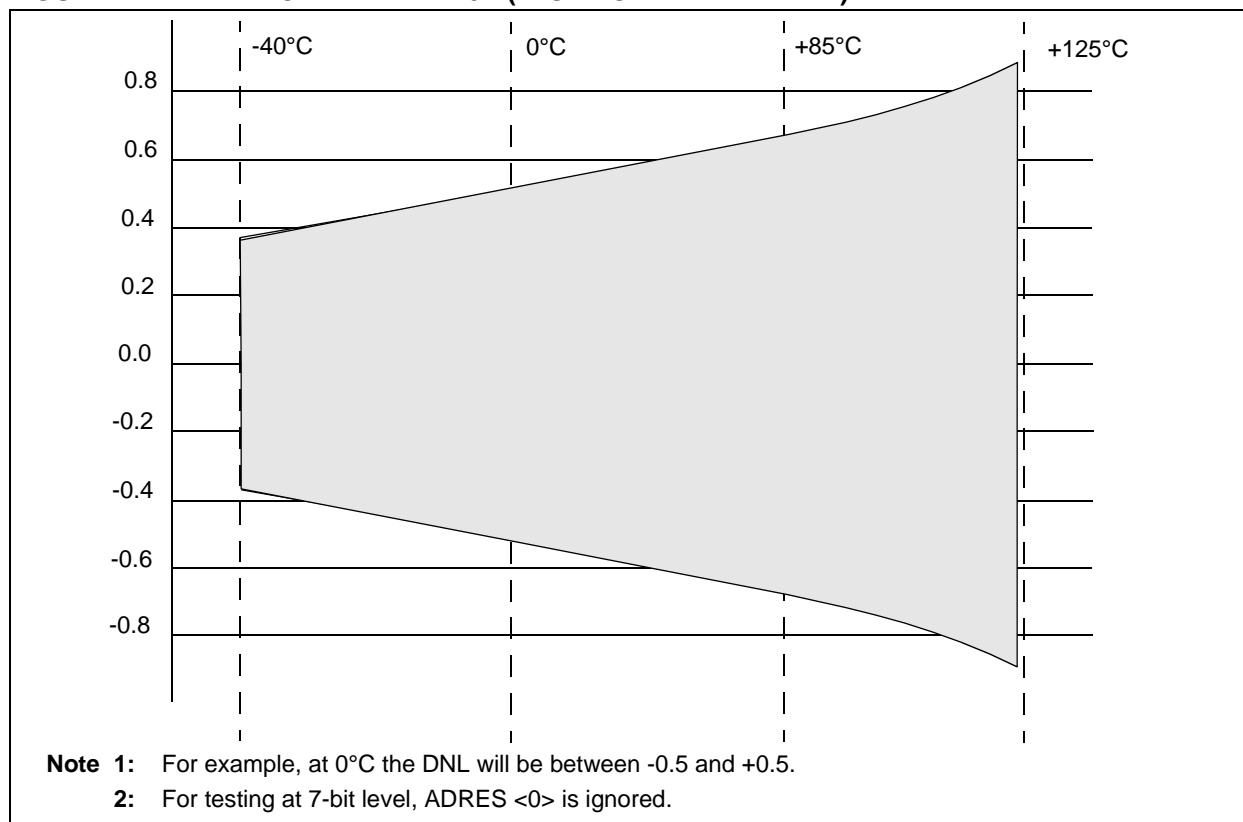
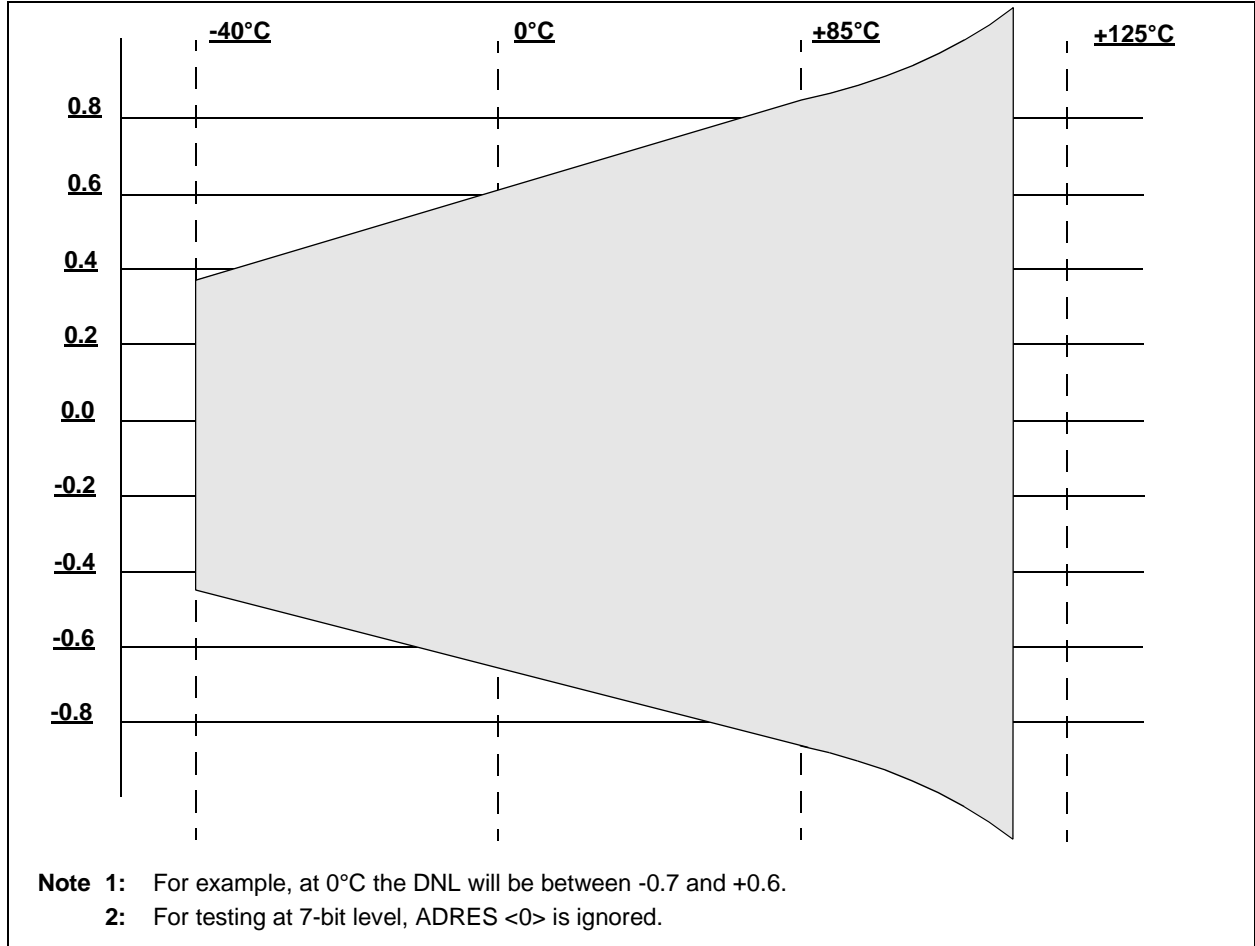


FIGURE 2: TYPICAL DNL AT 5.5V (TESTING AT 7-BIT LEVEL)



Work around:

None.

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Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41270B), the following clarifications and corrections should be noted.

None.

APPENDIX A: REVISION HISTORY

Rev A Document (04/2006)

First revision of this document. Covers ADC.

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