ALPHA & OMEGA SEMICONDUCTOR

AOC4810

30V Common-Drain Dual N-Channel MOSFET

General Description

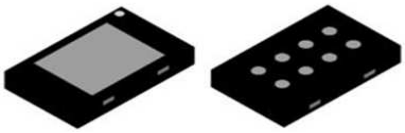
The AOC4810 uses advanced trench technology to provide excellent $R_{SS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V while retaining a 20V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration.

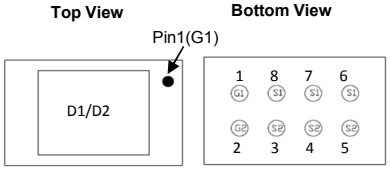
Product Summary

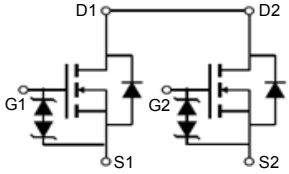
Vss	30V
I_S (at V_{GS}=10V)	8A
$R_{SS(ON)}$ (at V_{GS}=10V)	< 8.8mΩ
$R_{SS(ON)}$ (at V_{GS}=4.5V)	< 14.5mΩ
Typical ESD protection	**HBM Class 3A**

Green Product

AlphaDFN 3.2x2_8







Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{SS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Source Current (DC) Note1	T_A=25°C	I_S	8	A
Source Current (Pulse) Note2		I_{SM}	30	
Power Dissipation Note1	T_A=25°C	P_D	0.9	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient	t ≤ 10s	$R_{\theta JA}$	75	90	°C/W
Maximum Junction-to-Ambient	Steady-State		120	145	°C/W

Note 1. Mounted on minimum pad PCB.

Note 2. PW <300 µs pulses, duty cycle 0.5% max

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{SSS}	Source-Source Breakdown Voltage	I_S=250µA, V_{GS}=0V, Test Circuit 6	30			V
I_{SSS}	Zero Gate Voltage Source Current	V_{SS}=30V, V_{GS}=0V, Test Circuit 1			1	µA
		T_J=55°C			5	
I_{GSS}	Gate leakage current	V_{SS}=0V, V_{GS}= ±16V, Test Circuit 2			±10	
$V_{GS(th)}$	Gate Threshold Voltage	V_{SS}=$V_{GS,}$ I_S=250µA, Test Circuit 3	1.4	1.8	2.2	V
$R_{SS(ON)}$	Static Source to Source On-Resistance	V_{GS}=10V, I_S=5A, Test Circuit 4		7.2	8.8	mΩ
		T_J=125°C		10	12.2	
		V_{GS}=4.5V, I_S=5A, Test Circuit 4		11.5	14.5	
g_{FS}	Forward Transconductance	V_{SS}=5V, I_S=5A, Test Circuit 3		25		S
V_{FSS}	Diode Forward Voltage	I_S=1A,V_{GS}=0V, Test Circuit 5		0.71	1	V
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz,		1130		pF
C_{oss}	Output Capacitance			500		pF
C_{rss}	Reverse Transfer Capacitance			90		pF
R_g	Gate resistance	V_{GS}=0V, V_{SS}=0V, f=1MHz		1.1		Ω
SWITCHING PARAMETERS						
$t_{D(on)}$	Turn-On DelayTime	V_{G1S1}=10V, V_{SS}=15V, R_L=3Ω, R_{GEN}=3Ω		8		ns
t_r	Turn-On Rise Time			16		ns
$t_{D(off)}$	Turn-Off DelayTime			25		ns
t_f	Turn-Off Fall Time			5		ns
Q_g	Total Gate Charge	V_{G1S1}=10V, V_{SS}=15V, I_S=5A		20		nC

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

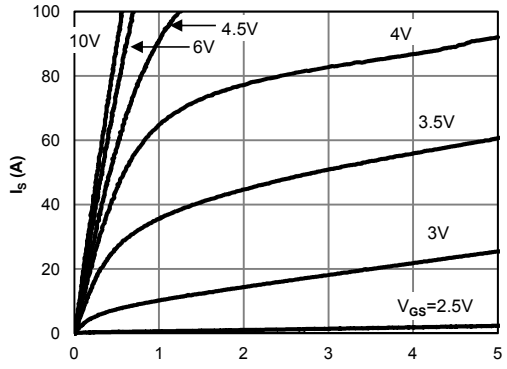


Fig 1: On-Region Characteristics

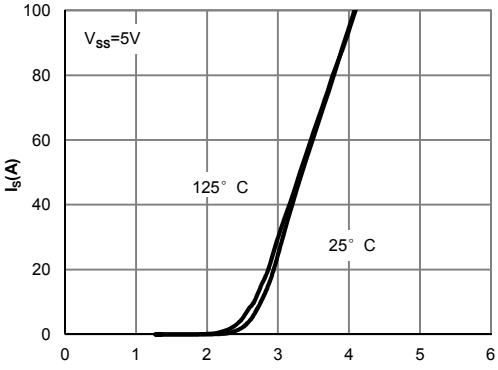


Figure 2: Transfer Characteristics

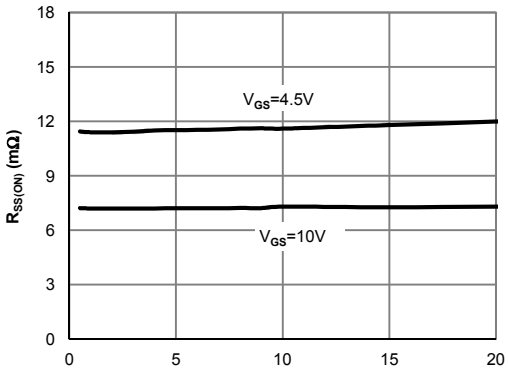


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

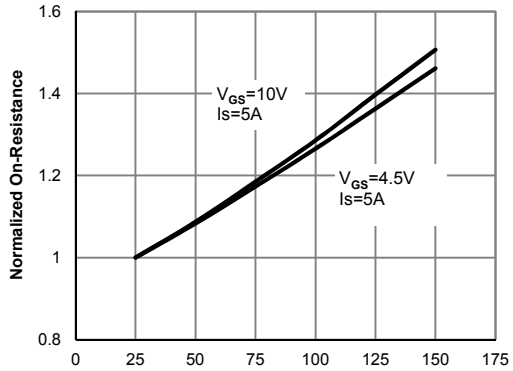


Figure 4: On-Resistance vs. Junction Temperature

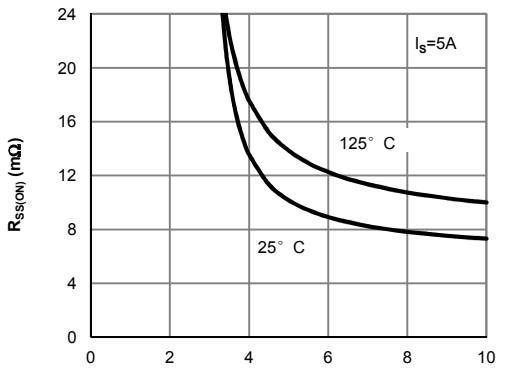


Figure 5: On-Resistance vs. Gate-Source Voltage

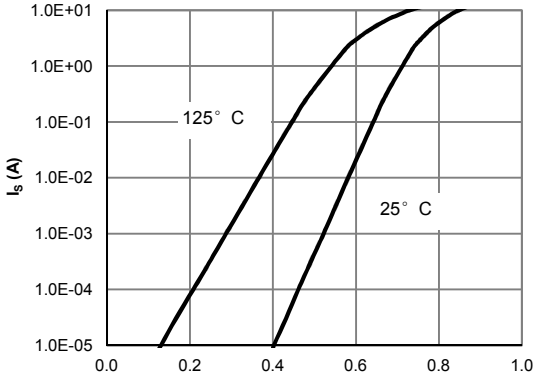


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

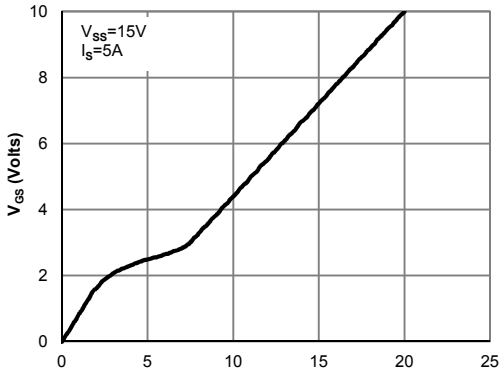


Figure 7: Gate-Charge Characteristics

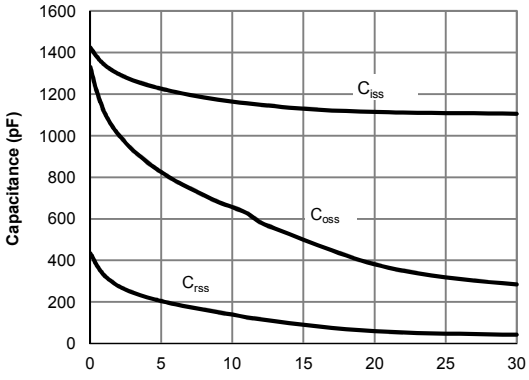
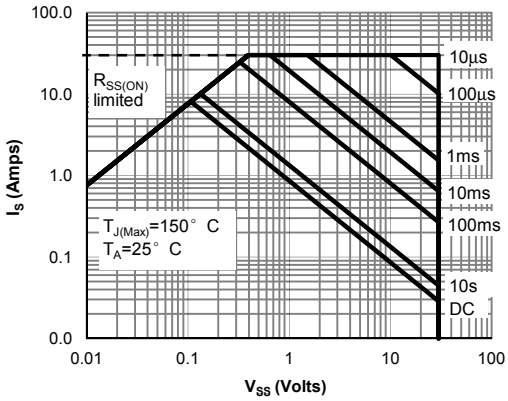


Figure 8: Capacitance Characteristics



VGS> or equal to 4.5V

Figure 9: Maximum Forward Biased Safe

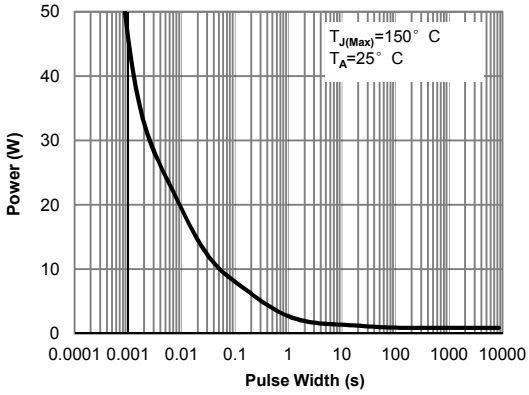


Figure 10: Single Pulse Power Rating Junction-to-Ambient

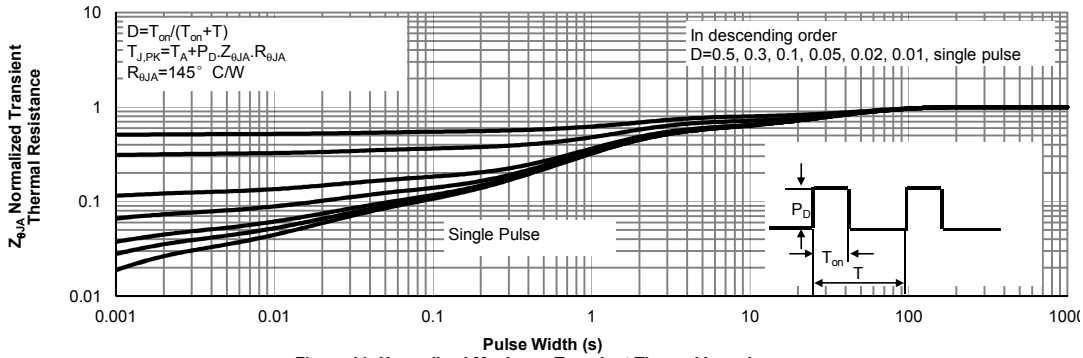
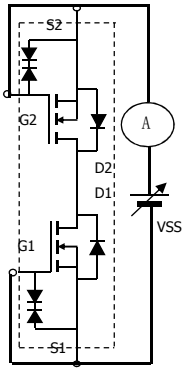


Figure 11: Normalized Maximum Transient Thermal Impedance

TEST CIRCUIT 1 Isss

POSITIVE VSS FOR ISSS+

NEGATIVE VSS FOR ISSS-

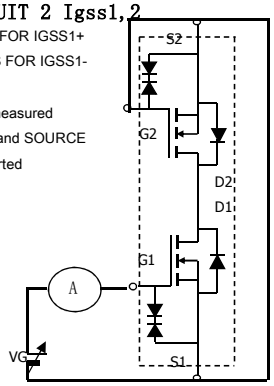


TEST CIRCUIT 2 Igss1,2

POSITIVE VGS FOR IGSS1+

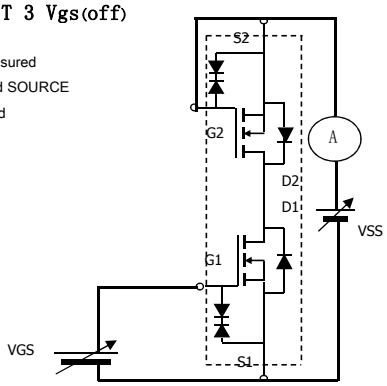
NEGATIVE VGS FOR IGSS1-

When FET1 is measured between GATE and SOURCE of FET2 are shorted



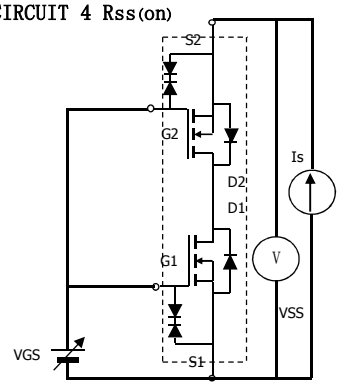
TEST CIRCUIT 3 Vgs(off)

When FET1 is measured between GATE and SOURCE of FET2 are shorted



TEST CIRCUIT 4 Rss(on)

Vss/Is

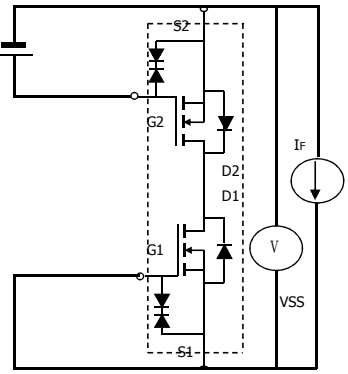


TEST CIRCUIT 5 $V_{F(SS)1,2}$

4.5V

When FET1 measured FET2 VGS=4.5V

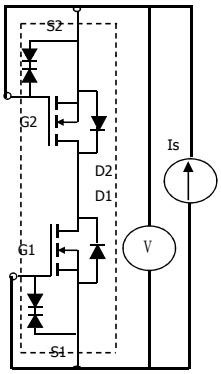
VGS=0



TEST CIRCUIT 6 BV_{DSS}

POSITIVE VSS FOR ISSS+

NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 7 $BV_{GS01,2}$

POSITIVE VSS FOR ISSS+

NEGATIVE VSS FOR ISSS-

When FET1 is measured between GATE and SOURCE of FET2 are shorted