



STC6NF30V

N-channel 30V - 0.020Ω - 6A - TSSOP8
2.5V-drive STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STC6NF30V	30V	< 0.025 Ω (@ 4.5 V) < 0.030 Ω (@ 2.7 V)	6A

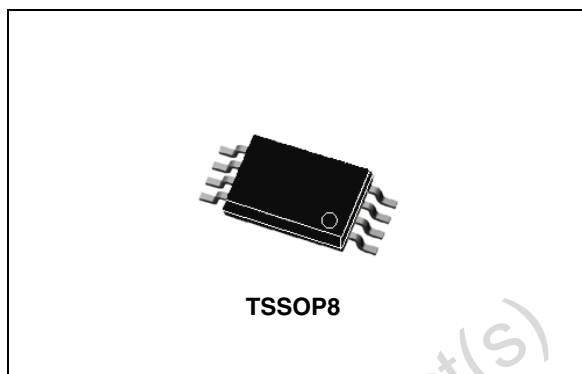
- Ultra low threshold gate drive (2.5V)
- Standard outline for easy automated surface mount assembly
- Double dice in common drain configuration

Description

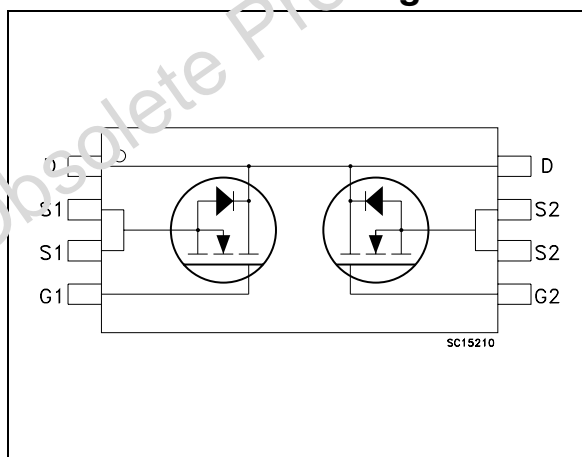
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance.

Applications

- Switching application



Internal schematic diagram



Order code

Part number	Marking	Package	Packaging
STC6NF30V	C6NF30V	TSSOP8	Tape & reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuit	9
4	Package mechanical data	10
5	Revision history	12

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	20	V
V_{GS}	Gate-source voltage	± 12	V
I_D	Drain current (continuous) at $T_C = 25^\circ C$	6	A
I_D	Drain current (continuous) at $T_C = 100^\circ C$	3.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at $T_C = 25^\circ C$	1.5	W
T_{stg}	Storage temperature	-55 to 150	$^\circ C$
T_J	Max. Operating Junction Temperature	-55 to 150	$^\circ C$

1. Pulse width limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJ-PBC}$	Thermal resistance junction-PBC Max	100 ⁽¹⁾	$^\circ C/W$
$R_{thJ-PBC}$	Thermal resistance junction-PBC Max	83.5 ⁽²⁾	$^\circ C/W$

1. When Mounted on FR-4 board with 1 inch² pad, 2 oz. of Cu. and $t = 10$ sec.

2. When Mounted on minimum recommended footprint

2 Electrical characteristics

($T_J = 25^\circ\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @ } 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 12\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	0.6			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5\text{V}$, $I_D = 3\text{A}$ $V_{GS} = 2.5\text{V}$, $I_D = 3\text{A}$		0.020 0.025	0.025 0.030	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10\text{V}$, $I_D = 6\text{A}$		18		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		800		pF
C_{oss}	Output capacitance			180		pF
C_{rss}	Reverse transfer capacitance			32		pF
Q_g	Total gate charge	$V_{DD} = 15\text{V}$, $I_D = 6\text{A}$		6.8	9	nC
Q_{gs}	Gate-source charge	$V_{GS} = 2.5\text{V}$		2.0		nC
Q_{gd}	Gate-drain charge	Figure 16 on page 9		3.4		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{V}$, $I_D = 3\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 2.5\text{V}$ Figure 14 on page 9		20		ns	
t_r	Rise time			25		ns	
$t_{d(off)}$	Turn-off delay time				32		ns
t_f	Fall time				13		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6A, V_{GS} = 0$			1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 6A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 15V, T_J = 150^\circ C$ <i>Figure 16 on page 9</i>		25		ns
Q_{rr}	Reverse recovery charge			21		μC
I_{RRM}	Reverse recovery current			1.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

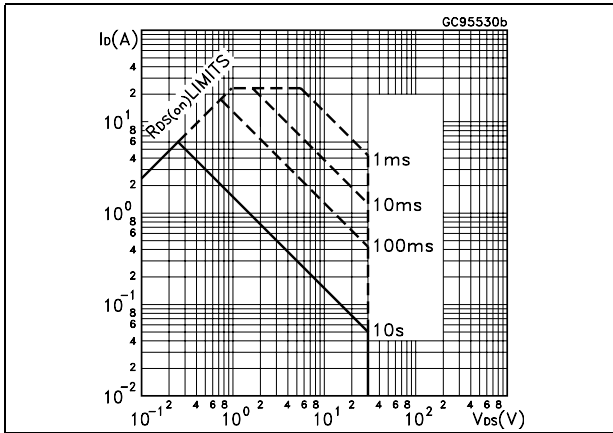


Figure 2. Thermal impedance

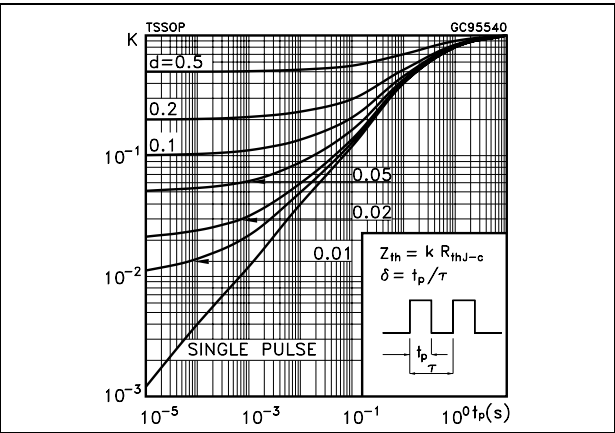


Figure 3. Output characteristics

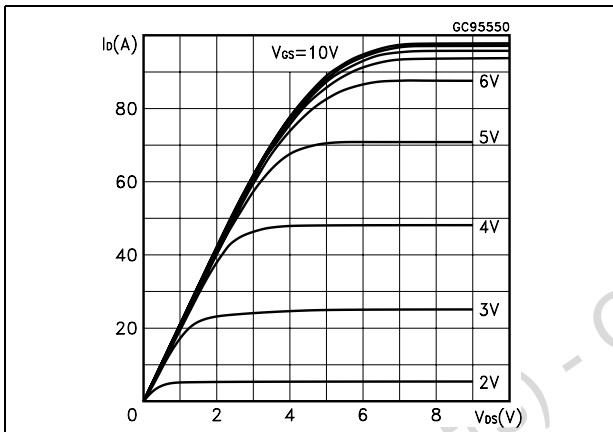


Figure 4. Transfer characteristics

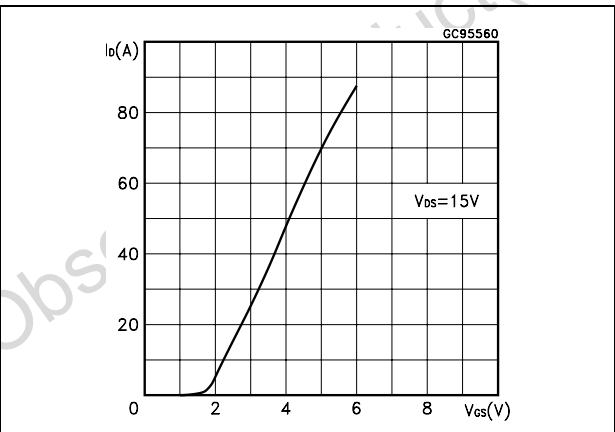


Figure 5. Transconductance

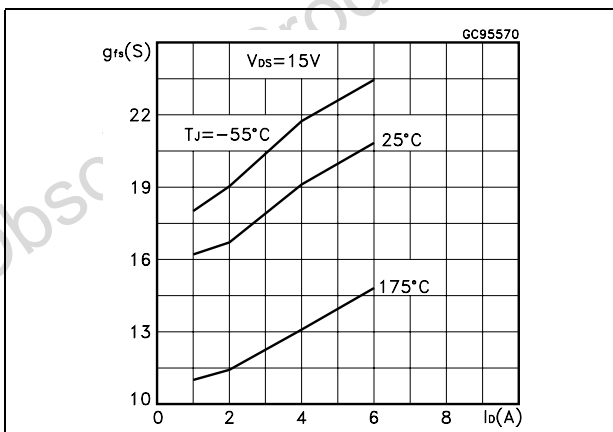


Figure 6. Static drain-source on resistance

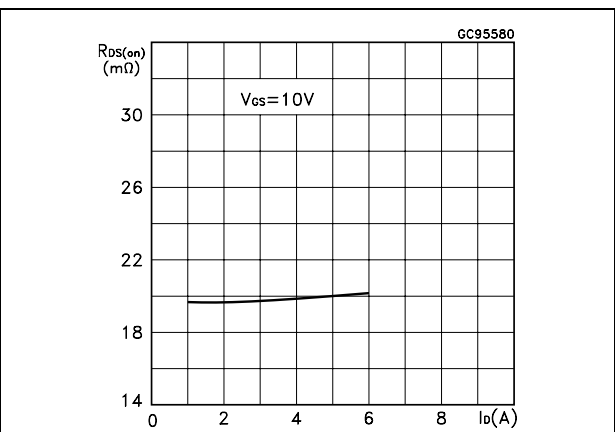


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

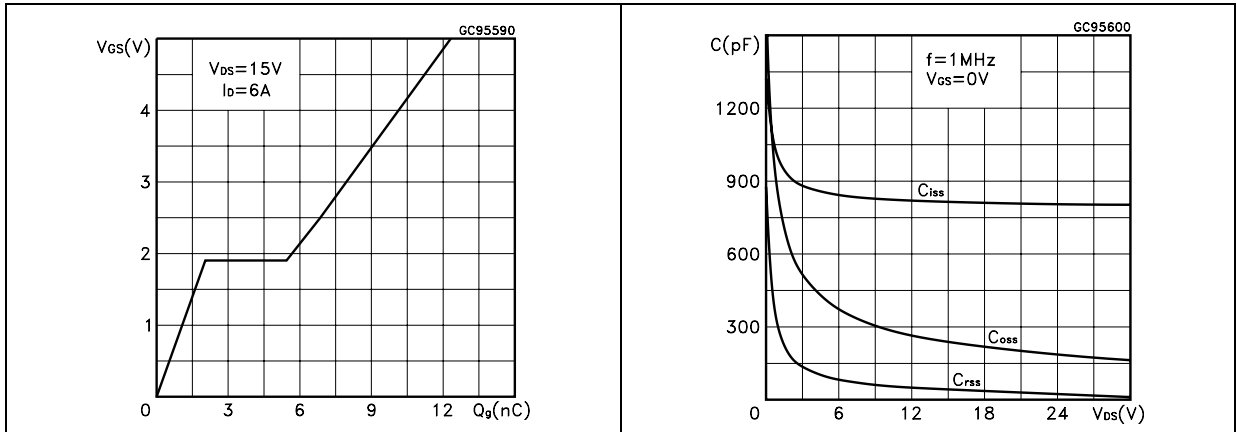


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

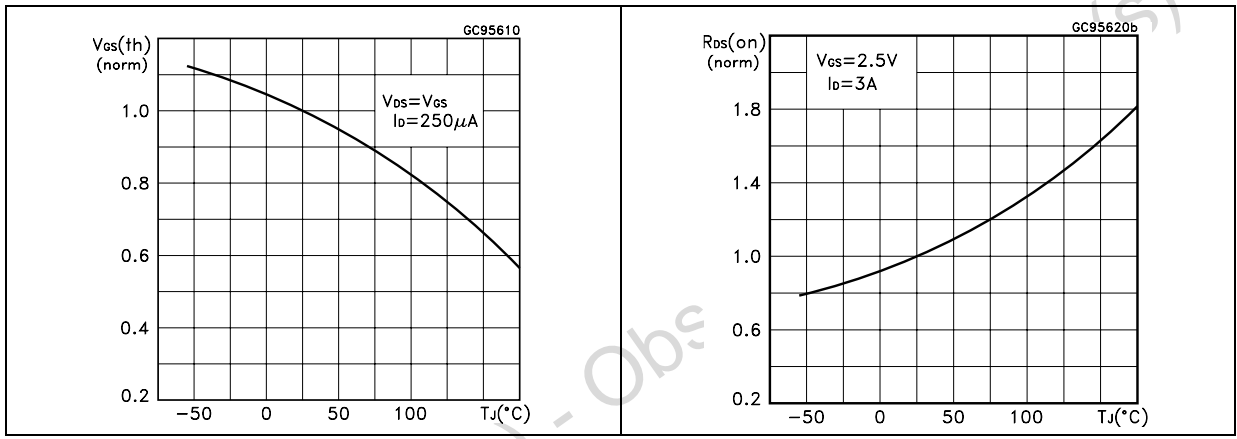


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage temperature

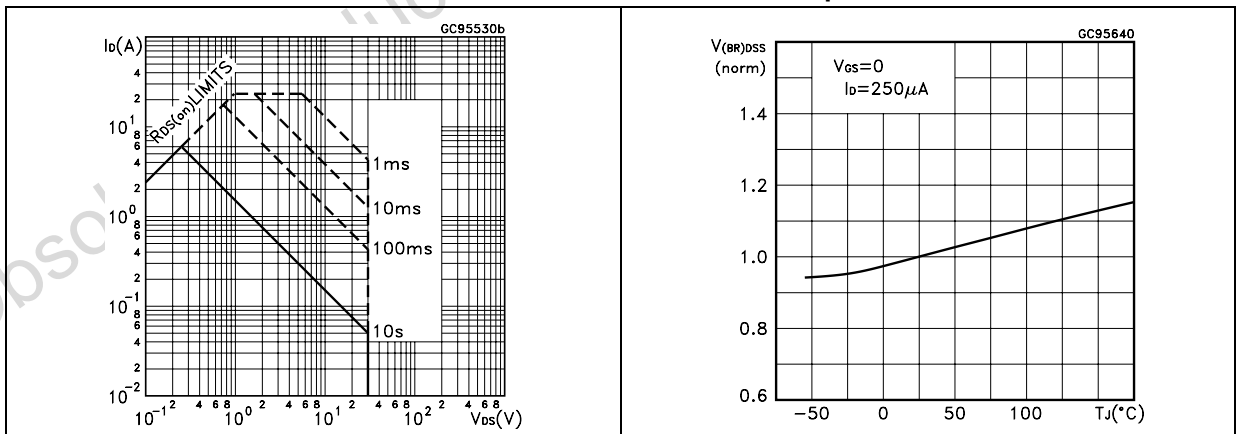
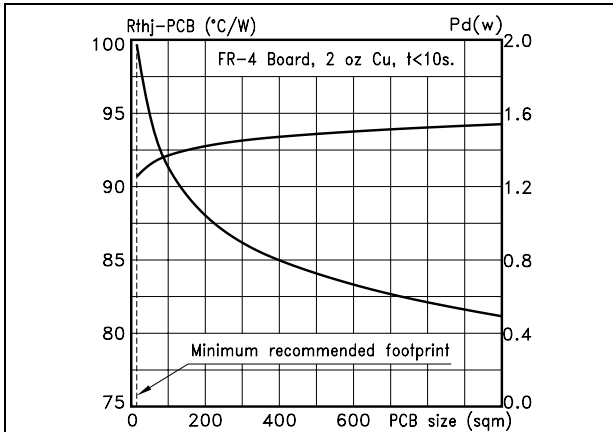


Figure 13. Thermal resistance and max power



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3 Test circuit

Figure 14. Switching times test circuit for resistive load

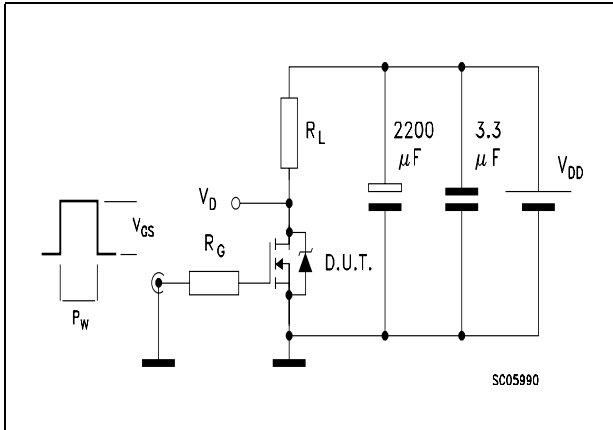


Figure 15. Gate charge test circuit

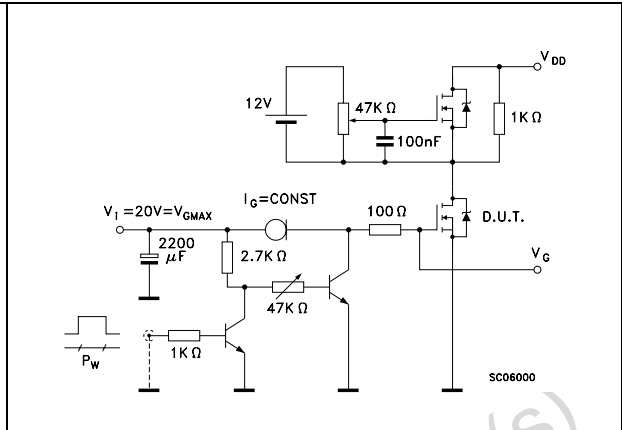
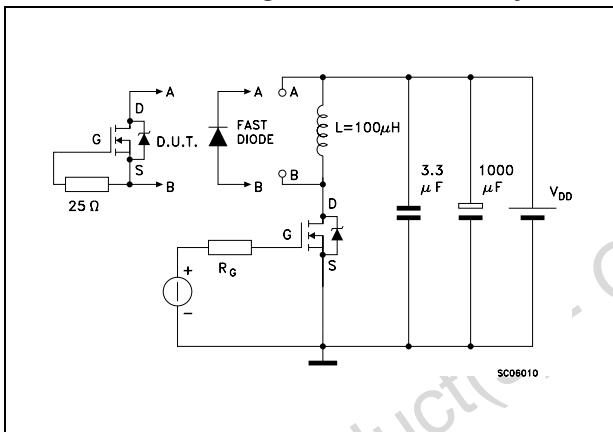


Figure 16. Test circuit for inductive load switching and diode recovery times



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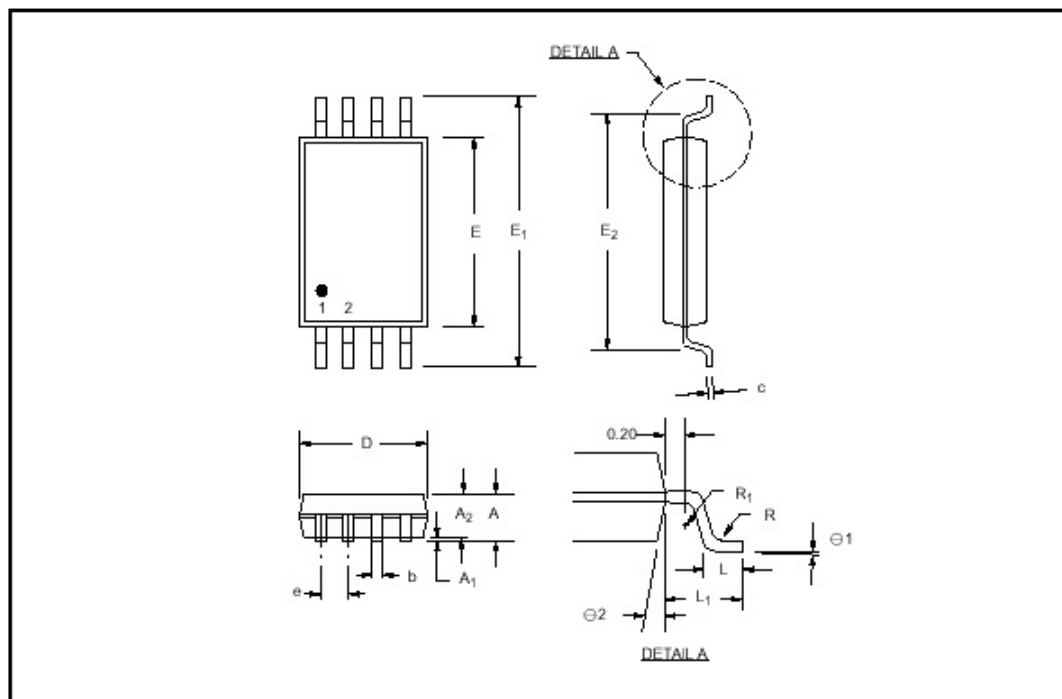
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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TSSOP8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.05		1.20	0.041		0.047
A1	0.05		0.15	0.002		0.006
A2	0.80		1.05	0.032		0.041
b	0.19		0.30	0.008		0.012
c		0.127			0.005	
D	2.90		3.10	0.114		0.122
E	4.30		4.50	0.170		0.177
E1	6.20		6.60	0.240		0.260
E2	5.14		5.24	0.202		0.206
e		0.65			0.025	
L	0.45		0.75	0.018		0.030
L1	0.90		1.10	0.0355		0.0433
R	0.09			0.004		
R1	0.09			0.004		
$\theta 1$	0°		8°	0°		8°
$\theta 2$	12°					



5 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	2	Complete document
03-Aug-2006	3	The document has been reformatted, SOA updated
01-Feb-2007	4	Typo mistake on first page

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