

## Features

- **ARM7TDMI® ARM® Thumb® Processor Core**
  - High Performance 32-bit RISC
  - High-density 16-bit Instruction set (Thumb)
  - Leader in MIPS/Watt
  - Embedded ICE (In Circuit Emulation)
- **16 Kbytes Internal SRAM**
- **Fully Programmable External Bus Interface (EBI)**
  - Maximum External Address Space of 6 Mbytes, Up to Four Chip Select Lines
- **8-level Priority, Vectored Interrupt Controller**
  - Three External Interrupts Including One Fast Interrupt Line
- **Ten Channel Peripheral Data Controller (PDC)**
- **57 Programmable I/O Lines**
- **Four 16-bit General Purpose Timers (GPT)**
  - Three Configurable Modes: Counter, PWM, Capture
  - Four External Clock Inputs, Three Multi-purpose I/O Pins per Timer
- **Four 16-bit Simple Timers (ST)**
- **Four Channel 16-bit Pulse Width Modulation (PWM)**
- **Four CAN Controllers 2.0A and 2.0B Full CAN**
  - One with 32 Buffers, Three with 16 Buffers
- **Two USARTs**
  - Support for J1587 and LIN Protocols
- **One Master/Slave SPI Interface**
  - 8 to 16-bit Programmable Data Length
  - Four External Serial Peripheral Chip Selects
- **Two 8-channel 10-bit Analog to Digital Converters (ADC)**
- **Two 16-bit Capture Modules (CAPT)**
- **Programmable Watch Timer (WT)**
- **Programmable Watchdog (WD)**
- **Power Management Controller (PMC)**
  - 32 kHz Oscillator, Main Oscillator and PLL
- **IEEE 1149.1 JTAG Boundary-scan on all Digital Pins**
- **Fully Static Operation: 0 Hz to 30 MHz at VDDCORE=3.3V, 85°C**
- **3.0V to 5.5V Operating Voltage Range**
- **3.0V to 3.6V Core, Memory and Analog Voltage Range**
- **-40° to +85°C Operating Temperature Range**
- **Available in a 176-lead LQFP Package**

## Description

The AT91SAM7A2 is based on the ARM7TDMI embedded processor. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption.

In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications.

The AT91SAM7A2 has a direct connection to off-chip memory, including Flash, through the fully programmable External Bus Interface.

An 8-level priority vectored Interrupt Controller in conjunction with the Peripheral Data Controller significantly improves the real time performance of the device. The device is manufactured using high-density CMOS technology.

By combining the ARM7TDMI processor with an on-chip SRAM, and a wide range of peripheral functions, including USART, SPI, CAN Controllers, Timer Counter and Analog-to-Digital Converters, on a monolithic chip, the AT91SAM7A2 is a powerful device that provides a flexible, cost-effective solution to many compute-intensive embedded control applications in the automotive and industrial world.



## AT91 ARM® Thumb®- based Microcontrollers

### AT91SAM7A2

## Summary

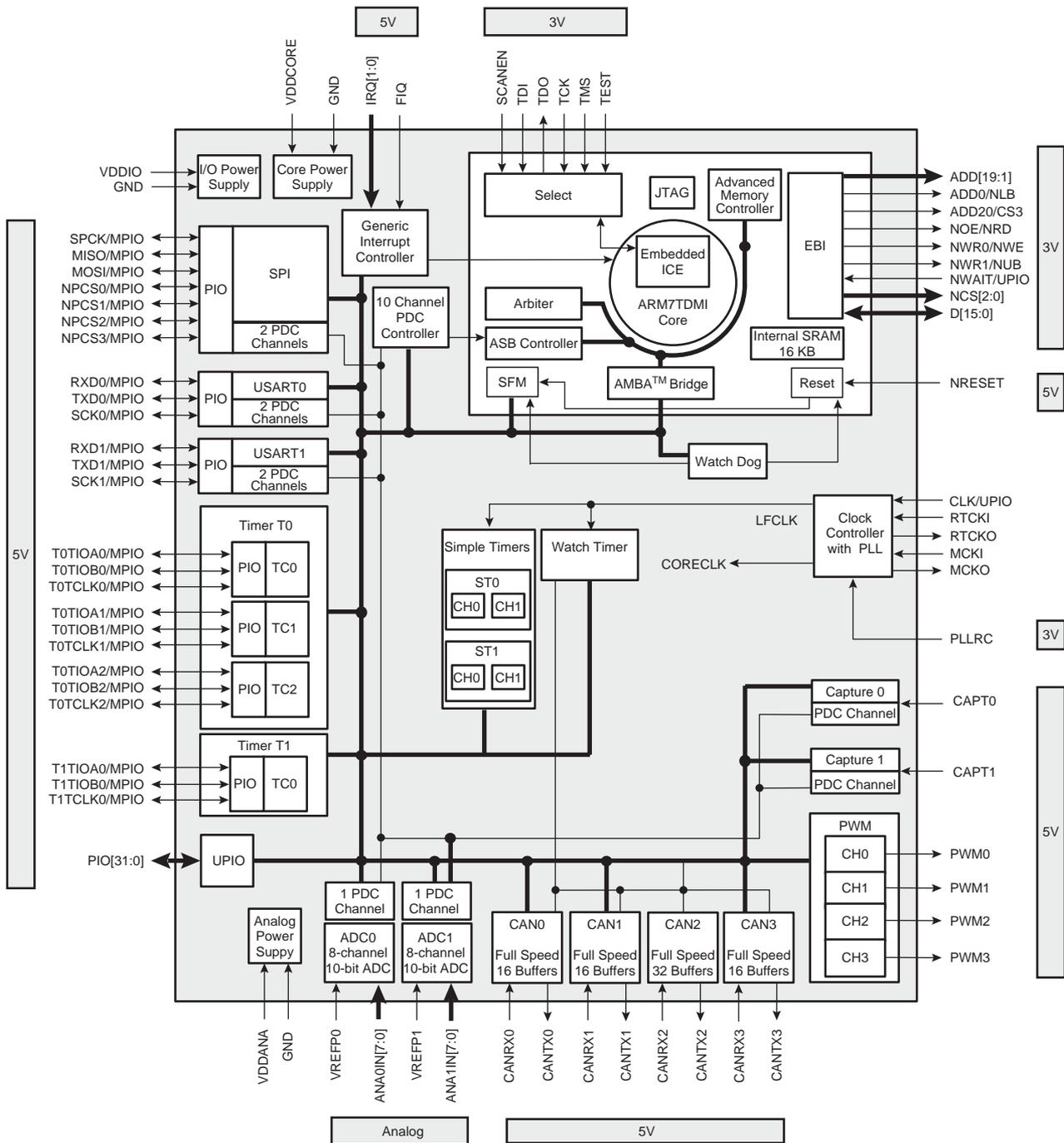
6021BS-ATARM-07/04



PRELIMINARY

# Block Diagram

Figure 1. Block Diagram

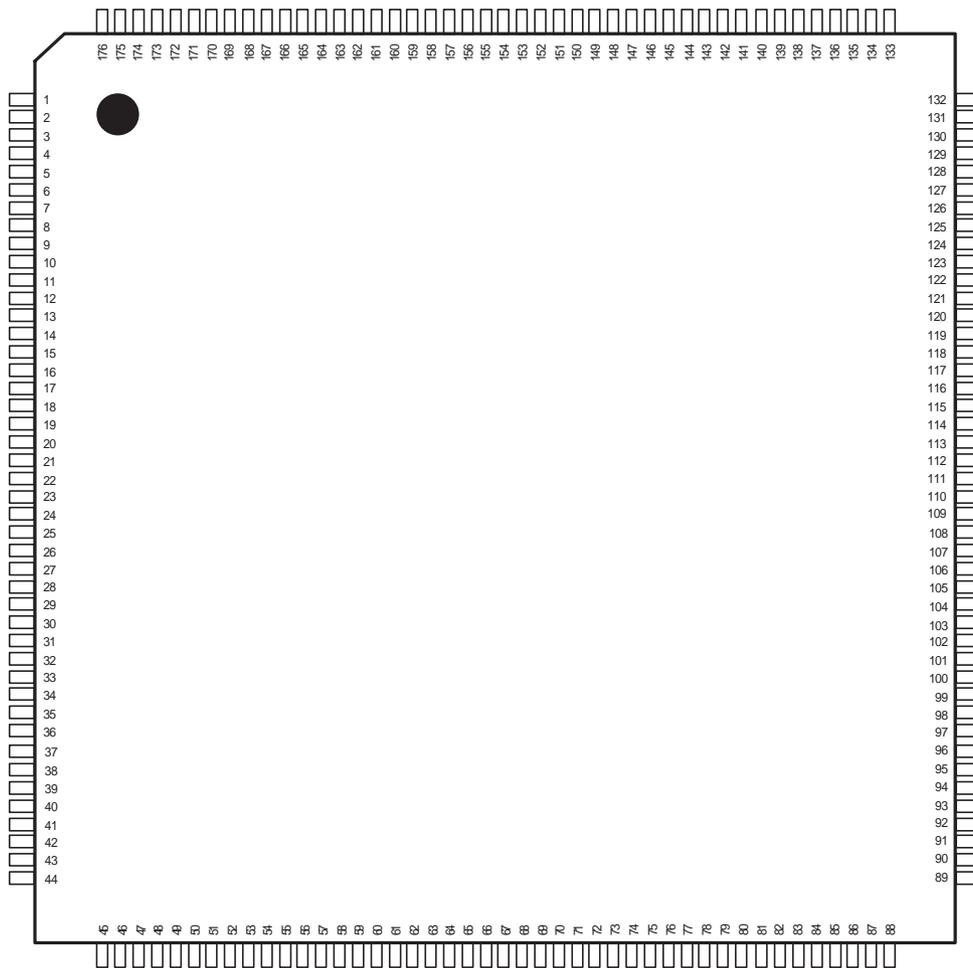


## Pin Configuration

Table 1. Pinout

| Pin | Name         | Pin | Name           | Pin | Name     | Pin | Name      |
|-----|--------------|-----|----------------|-----|----------|-----|-----------|
| 1   | VDDIO        | 45  | GND            | 89  | VDDIO    | 133 | NOE/NRD   |
| 2   | IRQ0         | 46  | VDDIO          | 90  | VDDANA   | 134 | NCS0      |
| 3   | IRQ1         | 47  | UPIO5          | 91  | VREFP0   | 135 | ADD1      |
| 4   | FIQ          | 48  | UPIO6          | 92  | ANA0IN0  | 136 | D9        |
| 5   | SCK0/MPIO    | 49  | GND            | 93  | ANA0IN1  | 137 | D2        |
| 6   | TXD0/MPIO    | 50  | VDDIO          | 94  | ANA0IN2  | 138 | VDDCORE   |
| 7   | RXD0/MPIO    | 51  | UPIO7          | 95  | ANA0IN3  | 139 | D10       |
| 8   | SCK1/MPIO    | 52  | UPIO 8         | 96  | ANA0IN4  | 140 | D3        |
| 9   | TXD1/MPIO    | 53  | UPIO 9         | 97  | ANA0IN5  | 141 | D11       |
| 10  | RXD1/MPIO    | 54  | UPIO 10        | 98  | ANA0IN6  | 142 | D4        |
| 11  | VDDCORE      | 55  | UPIO 11        | 99  | GND      | 143 | D12       |
| 12  | CANTX3       | 56  | UPIO 12        | 100 | VDDANA   | 144 | D5        |
| 13  | CANRX3       | 57  | UPIO 13        | 101 | ANA0IN7  | 145 | D13       |
| 14  | CAPT0        | 58  | UPIO 14        | 102 | VREFP1   | 146 | D6        |
| 15  | CAPT1        | 59  | UPIO 15        | 103 | ANA1IN0  | 147 | D14       |
| 16  | SPCK/MPIO    | 60  | UPIO 16        | 104 | ANA1IN1  | 148 | D7        |
| 17  | MISO/MPIO    | 61  | UPIO 17        | 105 | ANA1IN2  | 149 | D15       |
| 18  | MOSI/MPIO    | 62  | UPIO 18        | 106 | ANA1IN3  | 150 | GND       |
| 19  | NPCS0/MPIO   | 63  | GND            | 107 | ANA1IN4  | 151 | ADD0/NLB  |
| 20  | VDDIO        | 64  | VDDIO          | 108 | ANA1IN5  | 152 | ADD17     |
| 21  | GND          | 65  | UPIO19         | 109 | ANA1IN6  | 153 | ADD16     |
| 22  | NPCS1/MPIO   | 66  | UPIO20         | 110 | ANA1IN7  | 154 | ADD15     |
| 23  | NPCS2/MPIO   | 67  | UPIO21         | 111 | GND      | 55  | ADD14     |
| 24  | NPCS3/MPIO   | 68  | UPIO22         | 112 | VDDCORE  | 156 | ADD13     |
| 25  | T0TIOA0/MPIO | 69  | UPIO23         | 113 | RTCKI    | 157 | ADD12     |
| 26  | T0TIOB0/MPIO | 70  | UPIO24         | 114 | RTCKO    | 158 | ADD11     |
| 27  | T0TCLK0/MPIO | 71  | UPIO25         | 115 | GND      | 159 | ADD10     |
| 28  | T0TIOA1/MPIO | 72  | UPIO26         | 116 | VDDCORE  | 160 | ADD9      |
| 29  | T0TIOB1/MPIO | 73  | UPIO27         | 117 | SCANEN   | 161 | ADD20/CS3 |
| 30  | T0TCLK1/MPIO | 74  | UPIO28         | 118 | TEST     | 162 | VDDCORE   |
| 31  | T0TIOA2/MPIO | 75  | UPIO29         | 119 | TMS      | 163 | NWR0/NWE  |
| 32  | T0TIOB2/MPIO | 76  | UPIO30/NWAIT   | 120 | TDO      | 164 | NCS2      |
| 33  | VDDIO        | 77  | UPIO31/CORECLK | 121 | TDI      | 165 | NCS1      |
| 34  | GND          | 78  | CANTX0         | 122 | TCK      | 166 | ADD19     |
| 35  | T0TCLK2/MPIO | 79  | CANRX0         | 123 | GND      | 167 | ADD18     |
| 36  | T1TIOA0/MPIO | 80  | CANTX1         | 124 | PLLRC    | 168 | ADD8      |
| 37  | T1TIOB0/MPIO | 81  | CANRX1         | 125 | VDDCORE  | 169 | ADD7      |
| 38  | T1TCLK0/MPIO | 82  | CANTX2         | 126 | MCKI     | 170 | ADD6      |
| 39  | NRESET       | 83  | CANRX2         | 127 | MCKO     | 171 | ADD2      |
| 40  | UPIO0        | 84  | PWM0           | 128 | GND      | 172 | ADD3      |
| 41  | UPIO1        | 85  | PWM1           | 129 | NWR1/NUB | 173 | ADD4      |
| 42  | UPIO2        | 86  | PWM2           | 130 | D8       | 174 | ADD5      |
| 43  | UPIO3        | 87  | PWM3           | 131 | D1       | 175 | GND       |
| 44  | UPIO4        | 88  | GND            | 132 | D0       | 176 | GND       |

Figure 2. Pin Configuration



## Signal Description

Table 2. Signal Description

| Module           | Name               | Function   | Type | Active Level       | Comments   |   |
|------------------|--------------------|--|------|--------------------|--|---|
| EBI              | ADD[19:1]          | External address bus                             | O    | (Z) <sup>(1)</sup> | The EBI is tri-stated when NRESET is at a logical low level.<br>Internal pull-downs on data bus bits |   |
|                  | ADD0/NLB           | External address line line/<br>Lower byte enable | O    | L (Z)              |  |   |
|                  | ADD20/CS3          | External address line/ Chip select               | O    | H (Z)              |  |   |
|                  | D[15:0]            | External data bus                                | I/O  | (Z)                |  |   |
|                  | NOE                | Output enable                                    | O    | L (Z)              |  |   |
|                  | NWR0/NWE           | Write enable                                     | O    | L (Z)              |  |   |
|                  | NCS[2:0]           | Chip select lines                                | O    | L (Z)              |  |   |
|                  | NWR1/NUB           | Upper byte enable                                | O    | L (Z)              |  |   |
|                  | NWAIT              | External Wait                                    | I    | L                  |  | Disable at reset, multiplexed with UPIO30 |
|                  | CORECLK            | Core CLock                                       | O    |                    |  | Disable at reset, multiplexed with UPIO31 |
| GIC              | IRQ[1:0]           | External interrupt lines                         | I    |                    |  |   |
|                  | FIQ                | Fast interrupt line                              | I    |                    |  |   |
| Power-on Reset   | NRESET             | Hardware reset input                             | I    | L                  | Schmitt input with internal filter   |   |
| Master Clock     | MCKI               | Master clock input                               | I    |                    | Connected to external crystal (4 to 6 Mhz)   |   |
|                  | MCKO               | Master clock output                              | O    |                    |  |   |
|                  | PLLRC              | PLL RC network input                             | I    |                    |  |   |
| 32.768 kHz clock | RTCKI              | 32.768 KHz clock input                           | I    |                    | Connected to external 32.768 Khz crystal   |   |
|                  | RTCKO              | 32.768 KHz clock output                          | O    |                    |  |   |
| PIO              | UPIO[31:0]         | General purpose I/O                              | I/O  | (Z)                |  |   |
| USART0           | SCK0/MPIO          | USART0 clock line                                | I/O  | (Z)                | Multiplexed with general purpose I/O   |   |
|                  | RXD0/MPIO          | USART0 receive line                              | I/O  | (Z)                | Multiplexed with general purpose I/O   |   |
|                  | TXD0/MPIO          | USART0 transmit line                             | I/O  | (Z)                | Multiplexed with general purpose I/O   |   |
| USART1           | SCK1/MPIO          | USART1 clock line                                | I/O  | (Z)                | Multiplexed with general purpose I/O   |   |
|                  | RXD1/MPIO          | USART1 receive line                              | I/O  | (Z)                | Multiplexed with general purpose I/O   |   |
|                  | TXD1/MPIO          | USART1 transmit line                             | I/O  | (Z)                | Multiplexed with general purpose I/O   |   |
| Capture0         | CAPT0              | Capture input                                    | I    |                    |  |   |
| Capture1         | CAPT1              | Capture input                                    | I    |                    |  |   |
| PWM              | PWM[3:0]           | Pulse Width Modulation output                    | O    | (L)                |  |   |
| Timer T0         | T0TIOA[2:0]/MPIO   | Capture/waveform I/O                             | I/O  | (Z)                | Multiplexed with a general purpose I/O   |   |
|                  | T0TIOB[2:0]/MPIO   | Trigger/waveform I/O                             | I/O  | (Z)                | Multiplexed with a general purpose I/O   |   |
|                  | T0TIOCLK[2:0]/MPIO | External clock/trigger/input IO                  | I/O  | (Z)                | Multiplexed with a general purpose I/O   |   |

**Table 2.** Signal Description (Continued)

| Module         | Name           | Function                      | Type | Active Level | Comments  |
|----------------|----------------|-------------------------------|------|--------------|---|
| Timer T1       | T1TIOA/MPIO    | Capture/waveform I/O          | I/O  | (Z)          | Multiplexed with a general purpose I/O                  |
|                | T1TIOB/MPIO    | Trigger/waveform I/O          | I/O  | (Z)          | Multiplexed with a general purpose I/O                  |
|                | T0TIOCLK/MPIO  | External clock/trigger/input  | I/O  | (Z)          | Multiplexed with a general purpose I/O                  |
| ADC0           | ANA0IN[7:0]    | Analog input                  | I    |              |   |
|                | VREFP0         | Positive voltage reference    | I    |              |   |
| ADC1           | ANA1IN[7:0]    | Analog input                  | I    |              |   |
|                | VREFP1         | Positive voltage reference    | I    |              |   |
| SPI            | SPCK/MPIO      | SPI clock line                | I/O  | (Z)          | Multiplexed with a general purpose I/O                  |
|                | MISO/MPIO      | SPI master in slave out       | I/O  | (Z)          | Multiplexed with a general purpose I/O                  |
|                | MOSI/MPIO      | SPI master out slave in       | I/O  | (Z)          | Multiplexed with a general purpose I/O                  |
|                | NPCS[3:1]/MPIO | SPI chip select               | I/O  | (Z)          | Multiplexed with a general purpose I/O                  |
|                | NPCS0/NSS/MPIO | SPI chip select (slave input) | I/O  | (Z)          | Multiplexed with a general purpose I/O                  |
| CAN0           | CANRX0         | CAN0 receive line             | I    | L            |   |
|                | CANTX0         | CAN0 transmit line            | O    | L (H)        |   |
| CAN1           | CANRX1         | CAN1 receive line             | I    | L            |   |
|                | CANTX1         | CAN1 transmit line            | O    | L (H)        |   |
| CAN2           | CANRX2         | CAN2 receive line             | I    | L            |   |
|                | CANTX2         | CAN2 transmit line            | O    | L (H)        |   |
| CAN3           | CANRX3         | CAN3 receive line             | I    | L            |   |
|                | CANTX3         | CAN3 transmit line            | O    | L (H)        |   |
| JTAG           | SCANEN         | Scan enable                   | I    | H            | Internal pull-down (connected GND or leave unconnected) |
|                | TDI            | Test Data In                  | I    |              | Schmitt trigger, internal pull-up                       |
|                | TDO            | Test Data Out                 | O    |              |   |
|                | TMS            | Test Mode Select              | I    |              | Schmitt trigger, internal pull-up                       |
|                | TCK            | Test Clock                    | I    |              | Schmitt trigger, internal pull-up                       |
|                | TEST           | Factory Test                  | I    | H            | Internal pull-down (connected GND or leave unconnected) |
| Power Supplies | VDDCORE        | Core Power Supply             | -    |              | 3.3V  |
|                | VDDANA         | Analog Power Supply           | -    |              | 3.3V  |
|                | VDDIO          | I/O Lines Power Supply        | -    |              | 3.3V to 5V  |
|                | GND            | Ground                        | -    |              |   |

Note: 1. Values in brackets are the values at reset (H = High, L = Low, Z = High impedance state).

## Architectural Overview

The AT91SAM7A2 architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories and the external memories and devices by means of the External Bus Interface (EBI). The APB is designed for access to on-chip peripherals and is optimized for low power consumption. The AMBA™ Bridge provides an interface between the ASB and the APB.

The AT91SAM7A2 peripherals are designed to be programmed with a minimum number of instructions. Each peripheral has a 16 Kbyte address space allocated in the upper 1 Mbytes of the 4 Gbyte address space. Except for the interrupt controller, the peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status and interrupt registers. To maximize the efficiency of bit manipulation, frequently written registers are mapped into three memory locations. The first address is used to set the individual register bits, the second resets the bits and the third address reads the value stored in the register. A bit can be set or reset by writing a one to the corresponding position at the appropriate address. Writing a zero has no effect. Individual bits can thus be modified without having to use costly read-modify-write and complex bit manipulation instructions.

The ARM7TDMI processor operates in little-endian mode in the AT91SAM7A2 microcontroller. The processor's internal architecture and the ARM and Thumb instruction sets are described in the ARM7TDMI Datasheet.

## AMC: Advanced Memory Controller

The AT91SAM7A2 embeds 16 Kbytes of internal SRAM. The internal memory is directly connected to the 32-bit data bus and is single-cycle accessible. This provides maximum performance of 27 MIPS @ 30 MHz by using the ARM instruction set of the processor, minimizing system power consumption and improving on the performance of separate memory solutions.

## EBI: External Bus Interface

The EBI generates the signals which control the accesses to the external memories or peripheral devices. The EBI is fully programmable and can address up to 6 Mbytes. It has four chip selects and a 21-bit address bus, the upper bit of which is multiplexed with a chip select. Separate read and write control signals allow for direct memory and peripheral interfacing. The EBI supports different access protocols allowing single clock cycle memory accesses. The main features are:

- External Memory Mapping
- Up to Four Chip Select Lines
- Byte Write or Byte Select Lines
- 8-bit or 16-bit Data Bus
- External Wait
- Remap of Boot Memory
- Two Different Read Protocols
- Programmable Wait State Generation

## GIC: Generic Interrupt Controller

The AT91SAM7A2 has an 8-level priority, individually maskable, vectored interrupt controller. This feature substantially reduces the software and real time overhead in handling internal and external interrupts. The interrupt controller is connected to the nFIQ (fast interrupt request) and the nIRQ (standard interrupt request) inputs of the ARM7TDMI™ processor. The processor's nFIQ line can only be asserted by the external fast interrupt request input: FIQ. The nIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the external interrupt request lines: IRQ0 to IRQ1. An 8-level priority encoder allows the customer to define the priority between the different nIRQ interrupt sources. Internal sources are programmed to

be level sensitive or edge triggered. External sources can be programmed to be positive or negative edge triggered or high or low level sensitive.

### **PIO: Parallel I/O Controller**

The AT91SAM7A2 has 57 configurable I/O lines. 32 pins (United PIO) on the AT91SAM7A2 are dedicated as general purpose I/O pins (UPIO0 to UPIO31). Other I/O lines are multiplexed with an external signal of a peripheral to optimize the use of available package pins. The United-PIO is controlled by a dedicated module. The others pins are configure in each module.

### **PDC: Peripheral Data Controller**

An on-chip, 10-channel Peripheral Data Controller (PDC) transfers data between the on-chip peripherals and the on and off-chip memories without processor intervention. One PDC channel is connected to the receiving channel and one to the transmitting channel of each USART and of the SPI. A single PDC channel is connected to each ADC and each Capture.

Most importantly, the PDC removes the processor interrupt handling over-head and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64 Kbytes without reprogramming the starting address. As a result, the performance of the micro-controller is increased and the power consumption reduced.

### **USART: Universal Synchronous Asynchronous Receiver Transmitter**

The AT91SAM7A2 provides two identical, full-duplex, universal synchronous asynchronous receiver transmitter which are connected to the Peripheral Data Controller. The main features are:

- Programmable Baud Rate Generator
- Parity, Framing and Overrun Error Detection
- Line Break Generation and Detection
- Automatic Echo, Local & Remote Loopback Modes
- Multi-drop Mode: Address Detection and Generation
- Interrupt Generation
- Two Dedicated Peripheral Data Controller Channels
- 5-, 6-, 7-, 8- and 9-bit Character Length
- Idle Flag for J1587 Protocol.
- Smart Card Transmission Error Feature
- Support LIN 1.2 Protocol with H/W Layer

### **SPI: Serial Peripheral Interface**

The AT91SAM7A2 features an SPI that provides communication with external devices in master or slave mode. The SPI has four external chip selects that can be connected to up to 15 devices. The data length is programmable from 8- to 16-bit.

As for the USART, a two-channel PDC is used to move data directly between memory and the SPI without CPU intervention for maximum real-time processing throughput.

### **CAN: Controller Area Network**

The AT91SAM7A2 provides four CANs (2.0A and 2.0B). These are based upon serial communications protocol which efficiently supports distributed real-time control with a very high level of security (one with 32 mailboxes and the others with 16 mailboxes).

The main features are:

- Prioritization of Messages
- Multi-master
- System Wide Data Consistency
- Error Detection and Error Signaling
- Automatic Retransmission Of Corrupted Messages

- Automatic Reply After Receive a Remote Frame
- Time Stamp on Each Transfer
- Multicast Reception with Time Synchronization
- Continuous Reception Mode

## **GPT: General Purpose Timer**

The AT91SAM7A2 features four General Purpose Timers. Each timer can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

Each General Purpose Timer has one external clock input, five internal clock inputs, and three multi-purpose input/output signals which can be configured by the user. Each timer drives an internal interrupt signal which can be programmed to generate processor interrupts via the AIC (Advanced Interrupt Controller).

Three General Purpose Timers are grouped in the same block. This block has two global registers which act upon all three GPTs. The Block Control Register allows the three timers to be started simultaneously with the same instruction. The Block Mode Register defines the external clock inputs for each timer, allowing them to be chained.

## **ST: Simple Timer**

Simple Timers provide basic functions for timing calculation. Each channel of this timer has a specific prescaler and a 16-bit counter. The prescaler defines the clock frequency of the channel counter. The 16-bit counter starts down-counting when a value different than zero is loaded. An interrupt is generated when the counter is null.

## **CAPT: Capture Module**

The capture module is a frame analyzer. It stores the period of time between two edges of a signal in a register. This period is described as a number of counter cycles. The capture allows data transfers with the PDC.

## **PWM: Pulse Width Modulation**

The AT91SAM7A2 includes four PWM channels. Each channel can generate pulses. The frequency and the duty cycle of each channel can be configured.

## **WT: Watch Timer**

The watch timer provides a seconds counter and an alarm function. The alarm register has a resolution of 30.5  $\mu$ s. This allows a 32-bit register to have sufficient range to cater for a 24 or 36 hour period.

## **WD: Watch Dog**

The AT91SAM7A2 has an internal watchdog which can be used to prevent system lock-up if the software becomes trapped in a deadlock.

## **SFM: Special Function Module**

The AT91SAM7A2 provides registers which implement the following special functions.

- Chip Identification
- RESET Status

**ADC: Analog to Digital Converter**

The two identical 8-channel 10-bit Analog-to-Digital Converters (ADC) are based on a Successive Approximation Register (SAR) approach. Each ADC has 8 analog input pins, ANA0IN0 to ANA0IN7 and ANA1IN0 to ANA1IN7, and provides an interrupt signal to the AIC. Both ADCs share the analog power supply pins  $V_{DDA}$  and  $GNDA$ , and the input reference voltage pin  $V_{REFP}$ . Each channel can be enabled or disabled independently, and has its own data register. The ADC can be configured to automatically enter Sleep Mode after a conversion sequence, and can be triggered by the software. The ADC allows a data transfer with the PDC.

**PMC: Power Management Controller**

The AT91SAM7A2 Power Management Controller allows optimization of power consumption. The PMC enables/disables the clock inputs of the PDC and ARM core. Moreover, the main oscillator, the PLL and the analog peripherals can be put in standby mode allowing minimum power consumption to be obtained. The PMC provides the following operating modes:

- Normal: the clock generator provides clock to chip.
- Wait Mode: the ARM core clock is deactivated.
- Slow Mode: the clock generator is deactivated, the system is clocked at 32.768 kHz.

Each peripheral clock can be independently stopped or started directly in the peripheral to further reduce power consumption in Normal, Wait and Slow Modes.

**ICE Debug Mode**

ARM Standard Embedded In Circuit Emulation is supported via the ICE port. It is connected to a host computer via an external ICE Interface. In ICE Debug Mode the ARM core responds with a non-JTAG chip ID which identifies the core to the ICE system. This is not JTAG IEEE 1149.1 compliant.

## Ordering Information

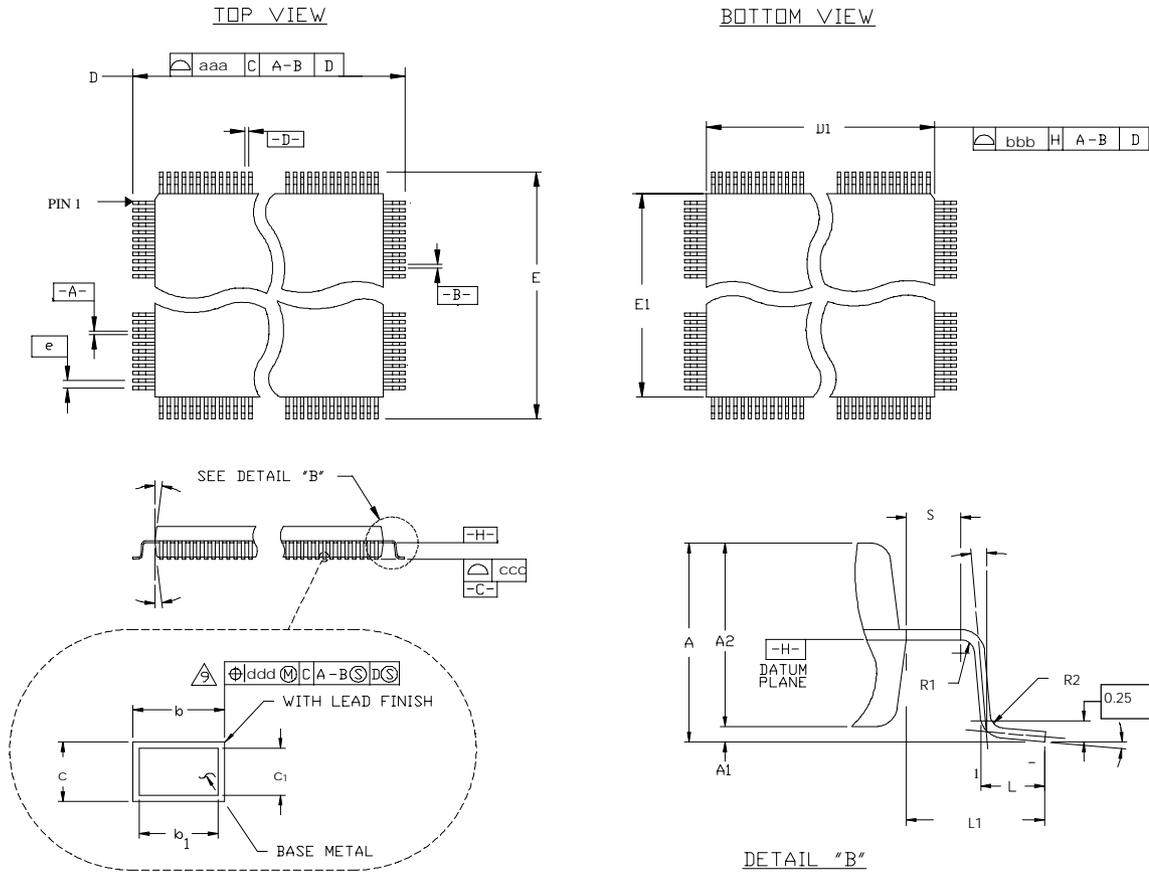
Table 3. Ordering Information

| Ordering Code | Package  | Temperature Operating Range    |
|---------------|----------|--------------------------------|
| AT91SAM7A2-AI | TQFP 176 | Industrial<br>(-40°C to +85°C) |

# Packaging Information

## Package Drawing

Figure 3. 176-lead LQFP Package Drawing



**Table 4.** Package Dimensions (mm)

| Symbol                                 | Min      | Nom  | Max  |
|--|----------|------|------|
| c                                      | 0.09     |      | 0.20 |
| c1                                     | 0.09     |      | 0.16 |
| L                                      | 0.45     | 0.6  | 0.75 |
| L1                                     | 1.00 REF |      |      |
| R2                                     | 0.08     |      | 0.2  |
| R1                                     | 0.08     |      |      |
| S                                      | 0.2      |      |      |
| q                                      | 0°       | 3.5° | 7°   |
| θ1                                     | 0°       |      |      |
| θ2                                     | 11°      | 12°  | 13°  |
| θ3                                     | 11°      | 12°  | 13°  |
| A                                      |          |      | 1.6  |
| A1                                     | 0.05     |      | 0.15 |
| A2                                     | 1.35     | 1.4  | 1.45 |
| <b>Tolerances of Form and Position</b> |          |      |      |
| aaa                                    |          | 0.2  |      |
| bbb                                    |          | 0.2  |      |

**Table 5.** Lead Count Dimensions (mm)

| Pin Count | D/E BSC | D1/E1 BSC | b    |      |      | b1   |      |      | e BSC | ccc  | ddd  |
|-----------|---------|-----------|------|------|------|------|------|------|-------|------|------|
|           |         |           | Min  | Nom  | Max  | Min  | Nom  | Max  |       |      |      |
| 176       | 26.0    | 24.0      | 0.17 | 0.20 | 0.27 | 0.17 | 0.20 | 0.23 | 0.50  | 0.10 | 0.08 |

**Table 6.** Device and 176-lead LQFP Package Maximum Weight

|      |    |
|------|----|
| 1900 | mg |
|------|----|

## Soldering Profile

Table 7 gives the recommended soldering profile from J-STD-20.

**Table 7.** Soldering Profile

|  | Convection or IR/Convection   | VPR                            |
|--|-------------------------------|--------------------------------|
| Average Ramp-up Rate (183°C to Peak)       | 3°C/sec. max.                 | 10°C/sec.                      |
| Preheat Temperature 125°C ±25°C            | 120 sec. max                  |                                |
| Temperature Maintained Above 183°C         | 60 sec. to 150 sec.           |                                |
| Time within 5°C of Actual Peak Temperature | 10 sec. to 20 sec.            | 60 sec.                        |
| Peak Temperature Range                     | 220 +5/-0°C or<br>235 +5/-0°C | 215 to 219°C or<br>235 +5/-0°C |
| Ramp-down Rate                             | 6°C/sec.                      | 10°C/sec.                      |
| Time 25°C to Peak Temperature              | 6 min. max                    |                                |

Small packages may be subject to higher temperatures if they are reflowed in boards with larger components. In this case, small packages may have to withstand temperatures of up to 235°C, not 220°C (IR reflow).

Recommended package reflow conditions depend on package thickness and volume. See Table 8 below.

**Table 8.** Recommended Package Reflow Conditions <sup>(1, 2, 3)</sup>

| Parameter     | Temperature  |
|---------------|--------------|
| Convection    | 220 +5/-0°C  |
| VPR           | 215 to 219°C |
| IR/Convection | 220 +5/-0°C  |

Notes: 1. The packages are qualified by Atmel by using IR reflow conditions, not convection or VPR.  
 2. By default, the package level 1 is qualified at 220°C (unless 235°C is stipulated).  
 3. The body temperature is the most important parameter but other profile parameters such as total exposure time to hot temperature or heating rate may also influence component reliability.

A maximum of three reflow passes is allowed per component.



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