

# PACDN004

## 2-Channel ESD Protection Array

### Product Description

The PACDN004 is a diode array designed to provide two channels of ESD protection for electronic components or sub-systems. Each channel consists of a pair of diodes which steers the ESD current pulse either to the positive ( $V_P$ ) or negative ( $V_N$ ) supply. The PACDN004 will protect against ESD pulses up to  $\pm 15$  kV Human Body Model, and  $\pm 8$  kV contact discharge per International Standard IEC 61000-4-2.

This device has identical characteristics as the PACDN006 (6-channel array). They can be used together in order to provide a larger number of protected inputs if required. This device is particularly well-suited for a wide range of portable electronics (e.g. cellular phones, PDAs, notebook computers) because of its small package footprint, high ESD protection level and low loading capacitance. It is also suitable for protecting video output lines and I/O ports in computers and peripherals.

The PACDN004 is available with RoHS compliant lead-free finishing.

### Features

- Two Channels of ESD Protection
- $\pm 8$  kV Contact,  $\pm 15$  kV Air ESD Protection per Channel (IEC 61000-4-2 Standard)
- $\pm 15$  kV of ESD Protection per Channel (HBM)
- Low Loading Capacitance of 3 pF Typical
- Low Leakage Current is Ideal for Battery-Powered Devices
- Miniature 4-Pin SOT-143 Package
- These Devices are Pb-Free and are RoHS Compliant

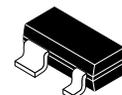
### Applications

- Consumer Electronic Products
- Cellular Phones
- PDAs
- Notebook Computers
- Desktop PCs
- Digital Cameras and Camcorders
- VGA (Video) Port Protection for Desktop and Portable PCs



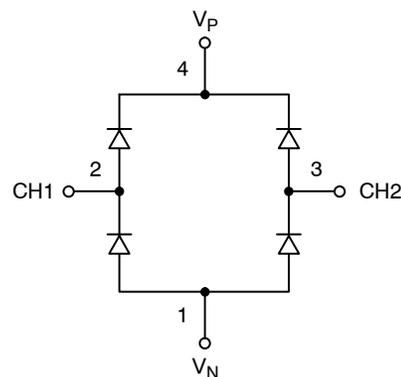
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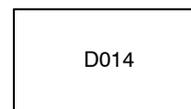


SOT-143  
SR SUFFIX  
CASE 527AF

### SIMPLIFIED ELECTRICAL SCHEMATIC



### MARKING DIAGRAM



D014 = PACDN004SR

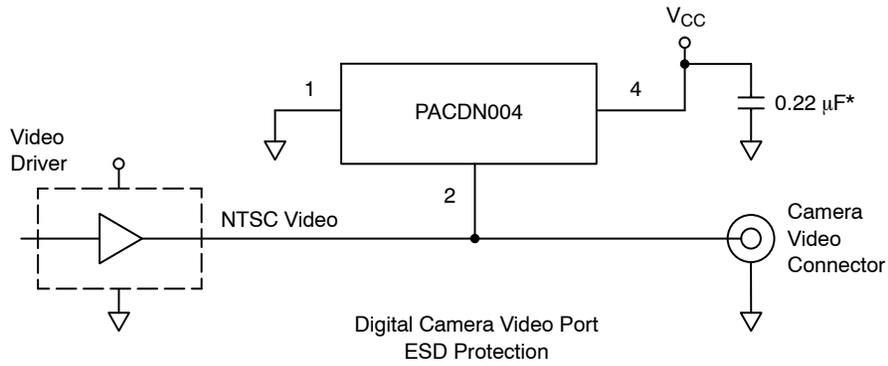
### ORDERING INFORMATION

Device	Package	Shipping†
PACDN004SR	SOT-143 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## TYPICAL APPLICATION CIRCUIT



\* Decoupling capacitor must be placed as close as possible to Pin4.

## PACKAGE / PINOUT DIAGRAM

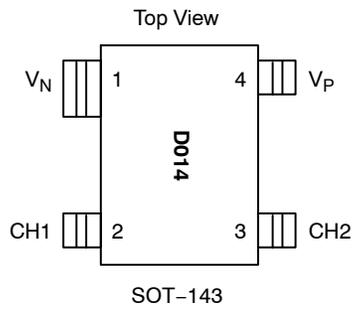


Table 1. PIN DESCRIPTIONS

PACDN004 (SOT-143)			
Pin	Name	Type	Description
1	V <sub>N</sub>	GND	Negative Voltage Supply Rail or Ground Reference Rail
2	CH1	I/O	ESD Channel 1
3	CH2	I/O	ESD Channel 2
4	V <sub>P</sub>	Supply	Positive Voltage Supply Rail

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## SPECIFICATIONS

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameter	Rating	Units
Supply Voltage ( $V_P - V_N$ )	6.0	V
Diode Forward DC Current (Note 1)	20	mA
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any Channel Input	$(V_N - 0.5)$ to $(V_P + 0.5)$	V
Package Power Rating	225	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Only one diode conducting at a time.

**Table 3. STANDARD OPERATING CONDITIONS**

Parameter	Rating	Units
Operating Temperature Range	-40 to +85	°C
Operating Supply Voltage ( $V_P - V_N$ )	0 to 5.5	V

**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_P$	Supply Current	$(V_P - V_N) = 5.5$ V			10	$\mu$ A
$V_F$	Diode Forward Voltage	$I_F = 20$ mA	0.65		0.95	V
$I_{LEAK}$	Channel Leakage Current			$\pm 0.1$	$\pm 1.0$	$\mu$ A
$C_{IN}$	Channel Input Capacitance	@ 1 MHz, $V_P = 5$ V, $V_N = 0$ V, $V_{IN} = 2.5$ V		3	5	pF
$V_{ESD}$	ESD Protection Peak Discharge Voltage at any Channel Input, in System a) Human Body Model, MIL-STD-883, Method 3015 b) Contact Discharge per IEC 61000-4-2 Standard c) Air Discharge per IEC 61000-4-2	(Note 2) (Notes 2 and 3) (Notes 2 and 4) (Notes 2 and 4)	$\pm 15$ $\pm 8$ $\pm 15$			kV
$V_{CL}$	Channel Clamp Voltage  Positive Transients Negative Transients	@ 15 kV ESD HBM (Notes 2 and 3)			$V_P + 13.0$ $V_N - 13.0$	V

1. All parameters specified at  $T_A = 25^\circ\text{C}$  unless otherwise noted.  $V_P = 5$  V,  $V_N = 0$  V unless noted.
2. From I/O pins to  $V_P$  or  $V_N$  only.  $V_P$  bypassed to  $V_N$  with a 0.22  $\mu$ F ceramic capacitor (see Application Information for more details).
3. Human Body Model per MIL-STD-883, Method 3015,  $C_{Discharge} = 100$  pF,  $R_{Discharge} = 1.5$  k $\Omega$ ,  $V_P = 5.0$  V,  $V_N$  grounded.
4. Standard IEC 61000-4-2 with  $C_{Discharge} = 150$  pF,  $R_{Discharge} = 330$   $\Omega$ ,  $V_P = 5.0$  V,  $V_N$  grounded.

PERFORMANCE INFORMATION

Input Capacitance vs. Input Voltage

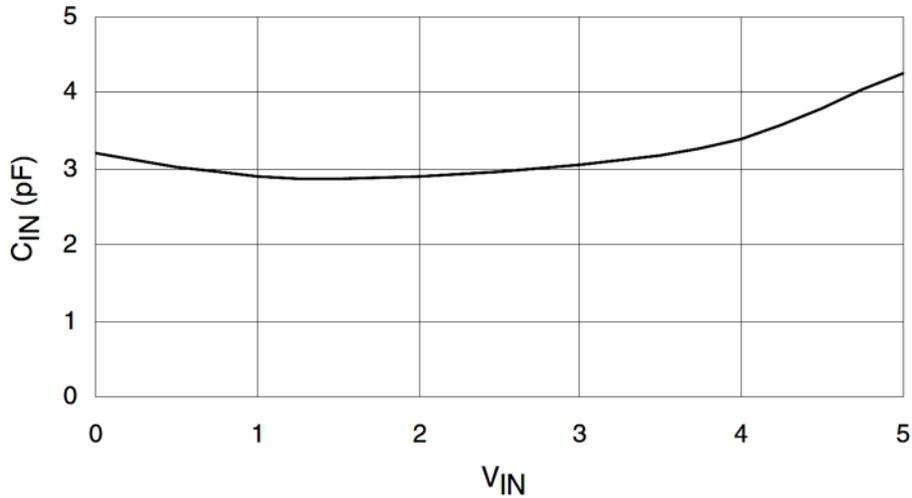


Figure 1. Typical Variation of C<sub>IN</sub> vs. V<sub>IN</sub>  
(V<sub>P</sub> = 5 V, V<sub>N</sub> = 0 V, 0.1 μF Chip Capacitor between V<sub>P</sub> and V<sub>N</sub>)

APPLICATION INFORMATION

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Application of Positive ESD Pulse between Input Channel and Ground, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L<sub>1</sub> and L<sub>2</sub>. The voltage V<sub>CL</sub> on the line being protected is:

$$V_{CL} = \text{Fwd Voltage Drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD})/dt + L_2 \times d(I_{ESD})/dt$$

where I<sub>ESD</sub> is the ESD current pulse, and V<sub>SUPPLY</sub> is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1 ns. Here d(I<sub>ESD</sub>)/dt can be approximated by ΔI<sub>ESD</sub>/Δt, or 30/(1x10<sup>-9</sup>). So just 10 nH of series inductance (L<sub>1</sub> and L<sub>2</sub> combined) will lead to a 300 V increment in V<sub>CL</sub>!

Similarly for negative ESD pulses, parasitic series inductance from the V<sub>N</sub> pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

Another consideration is the output impedance of the power supply for fast transient currents. Most power supplies exhibit a much higher output impedance to fast transient current spikes. In the V<sub>CL</sub> equation above, the V<sub>SUPPLY</sub> term, in reality, is given by (V<sub>DC</sub> + I<sub>ESD</sub> x R<sub>OUT</sub>), where V<sub>DC</sub> and R<sub>OUT</sub> are the nominal supply DC output voltage and effective output impedance of the power supply respectively. As an example, a R<sub>OUT</sub> of 1 Ω would result in a 10 V increment in V<sub>CL</sub> for a peak I<sub>ESD</sub> of 10 A.

If the inductances and resistance described above are close to zero, the rail-clamp ESD protection diodes will do a good job of protection. However, since this is not possible in practical situations, a bypass capacitor must be used to absorb the very high frequency ESD energy. So for any brand of rail-clamp ESD protection diodes, a bypass capacitor should be connected between the V<sub>P</sub> pin of the diodes and the ground plane (V<sub>N</sub> pin of the diodes) as shown in the Application Circuit diagram below. A value of 0.22 μF is adequate for IEC-61000-4-2 level 4 contact discharge protection (±8 kV). Ceramic chip capacitors mounted with short printed circuit board traces are good choices for this application. Electrolytic capacitors should be avoided as they have poor high frequency characteristics. For extra protection, connect a zener diode in parallel with the bypass capacitor to mitigate

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the effects of the parasitic series inductance inherent in the capacitor. The breakdown voltage of the zener diode should be slightly higher than the maximum supply voltage.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the  $V_P$  pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

### Additional Information

See also ON Semiconductor Application Notes AP209, "Design Considerations for ESD Protection" and AP219, "ESD Protection for USB 2.0 Systems".

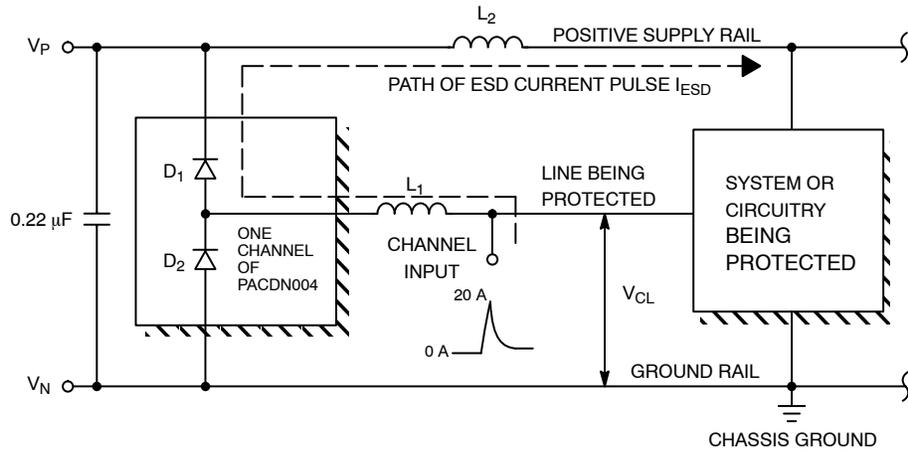
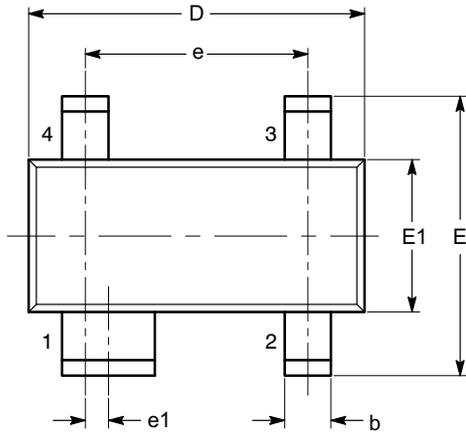


Figure 2. Application of Positive ESD Pulse between Input Channel and Ground

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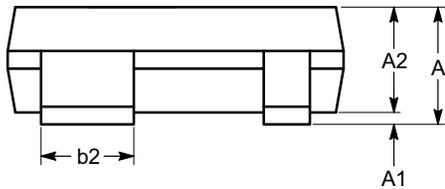
## PACKAGE DIMENSIONS

SOT-143, 4 Lead  
CASE 527AF-01  
ISSUE A

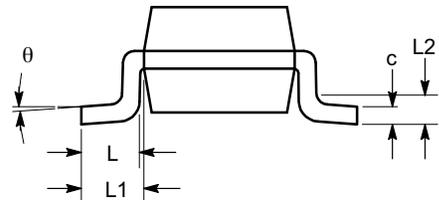


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.22
A1	0.05		0.15
A2	0.75	0.90	1.07
b	0.30		0.50
b2	0.76		0.89
c	0.08		0.20
D	2.80	2.90	3.04
E	2.10		2.64
E1	1.20	1.30	1.40
e	1.92 BSC		
e1	0.20 BSC		
L	0.40	0.50	0.60
L1	0.54 REF		
L2		0.25	
$\theta$	0°		8°



SIDE VIEW



END VIEW

### Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC TO-253.

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