i.MX Applications Processors

i.MX508 Processor for eReaders

Setting a new level of performance, reducing system cost and extending battery life

Overview

The i.MX508 is the first system-on-a-chip (SoC) designed specifically for eReaders that incorporates a high-performance 800 MHz ARM® Cortex™-A8 CPU and an integrated electronic paper display (EPD) controller, certified by E Ink® to drive current and next-generation Pearl™ panels. The i.MX508 enables reduced system cost, longer battery life and higher performance for faster page flips and a better reading experience.

Features

CPU Complex

- Up to 800 MHz ARM Cortex-A8 core
- 32 KB instruction and data caches
- Unified 256 KB L2 cache
- NEON™ SIMD media accelerator
- Vector floating point coprocessor

Multimedia

- OpenVG™ 1.1 hardware accelerator
- 32-bit primary display support up to SXGA+ resolution
- 16-bit secondary display support
- EPD controller supporting beyond 2048 × 1536 at 106 Hz refresh (or 4096 × 4096 at 20 Hz)
- Enhanced pixel processing pipeline (ePxP) supporting CSC, combine, rotate and gamma mapping

External Memory Interface

- Up to 2 GB LP-DDR2, DDR2 and LP-DDR1 (mDDR), 16/32-bit
- SLC/MLC NAND flash, 8/16-bit with 32-bit ECC

Advanced Power Management

- Multiple independent power domains
- State retention power gating (SRPG)
- Dynamic voltage and frequency scaling (DVFS)

Connectivity

- High-Speed USB 2.0 OTG with PHY
- High-Speed USB 2.0 Host with PHY

Controllers

- Wide array of serial interfaces, including SDIO, SPI, I²C and UART
- I²S audio interfaces
- 10/100 Ethernet controller

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Lower System Cost

The i.MX508 processor lowers system costs by as much as 50 percent over the cost of using a similar CPU with a stand-alone EPD display controller for Pearl panels. The i.MX508 integrates the following:

- E Ink-certified EPD controller to drive current and next-generation Pearl panels
- LCD controller to simultaneously drive small LCD screens in eReaders, or to connect with other eReader display technologies
- Ability to drive raw NAND flash memory up to 32-bit ECC
- Support for LP-DDR2, LP-DDR1 (mDDR) and DDR2 system memory
- Integrated USB 2.0 OTG controller and USB 2.0 host controller both with integrated PHYs

Performance

The i.MX508 provides for faster page turns and offers headroom for new features and applications. The i.MX508 features an 800 MHz ARM Cortex-A8 CPU with 256 KB of L2 cache for optimal PDF decode.

Other innovations for increased performance:

- Faster memory accesses due to 256 KB of L2 cache and a 64-bit AXI bus architecture
- An advanced pixel processing pipeline that performs common imaging algorithms like color space conversion, gamma mapping, rotation and scaling
- An integrated NEON DSP and OpenVG 2-D graphics accelerator for rapid decode of Adobe® PDF, Adobe Flash and other popular media formats

Extended Battery Life

Several aspects of the i.MX508 contribute to power savings:

- Quick file rendering and shutdown allows the Cortex-A8 CPU to offer a significantly higher performance/power ratio than slower CPUs that consume less active power
- The SoC supports current and next-generation, low-power LP-DDR2 memory

- The SoC was constructed with low-power transistors in the peripherals and high-performance transistors in the CPU
- The SoC has five independent power domains, each of which can be isolated while the other parts the SoC are running: CPU core, peripherals, memory, PLL, SRTC
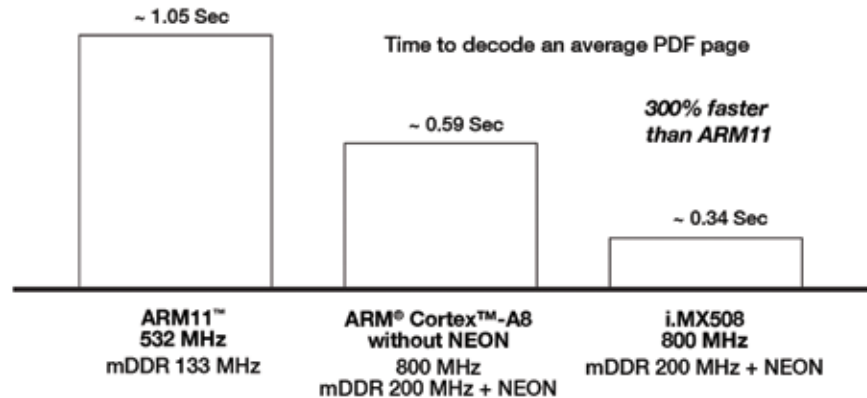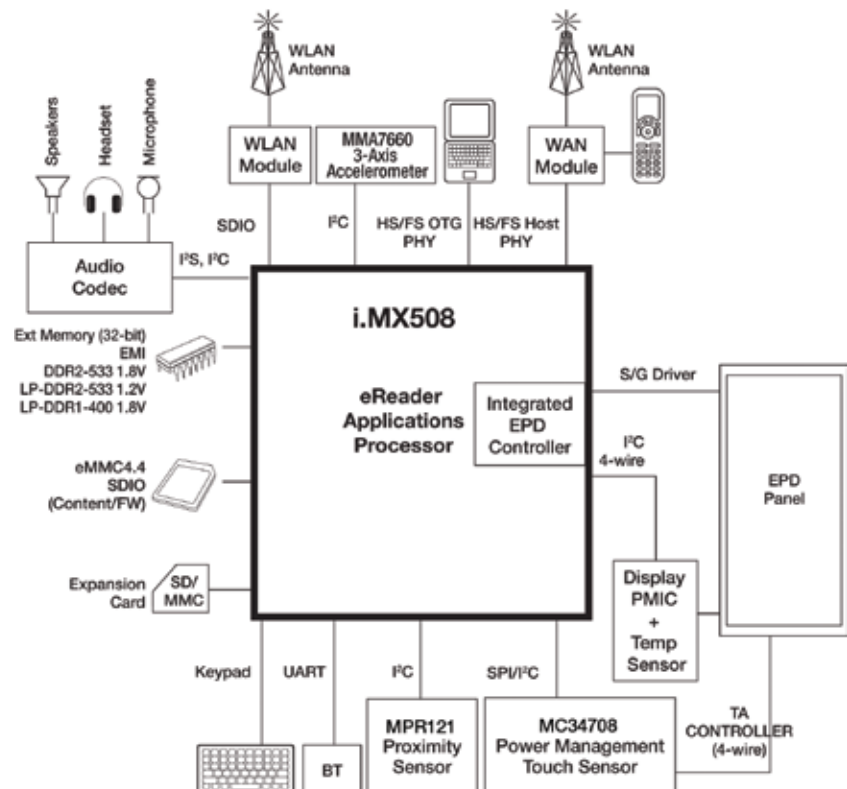
e-Reader System

Easier Development

Board support packages for the i.MX508 are available for the following operating systems:

- Linux®
- Android™

i.MX508 Performance
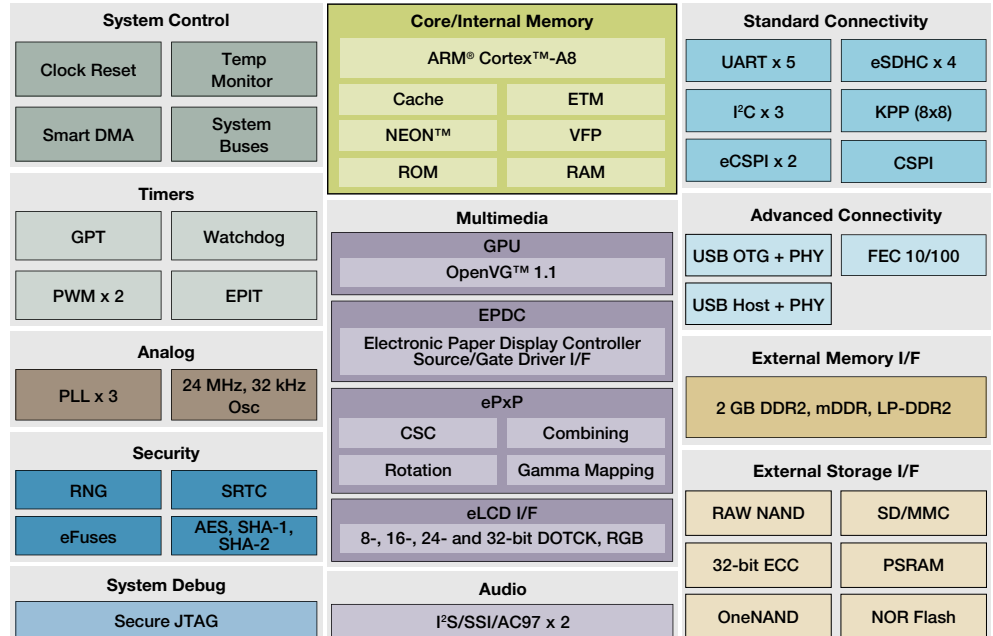

eReader System Diagram

E Ink-Certified EPD Controller

- High-performance, low-power pixel architecture
  - EPD TFT resolutions of 2048 x 1536 at 106 Hz refresh rate or 4096 x 4096 at 20 Hz
  - Allows support for dual scan style EPD TFT, which enables lower source driver clock frequencies while maintaining high refresh rates
- Tightly integrated with SoC memories and hardware acceleration modules
- Powerful and flexible programming model and driver architecture simplifies application software:
  - Support for up to 16 on-screen concurrent updates
  - Smart update processing minimizes memory bandwidth based on update region size
  - Each update region buffer can have an arbitrary location in memory (no need for physical display buffers)
  - Driver architecture encapsulates on-chip graphics hardware, pixel processor (CSC) and EPD controller to present a generic display interface to application software layers
- AXI bus interface to support multiple internal requestors to system memory, allowing efficient ordering at the memory controller
- Flexible TFT interface supports next-generation panel architectures

i.MX508 applications processor is designed for use with:

Part	Part Number	Design Manufacturer
Power Management IC	MC34708	Freescale
3-Axis, 12-bit Accelorometer	MMA8450Q	Freescale
Audio Codec with Headphone amp	SGTL5000	Freescale

i.MX508 Block Diagram

System Control
- Clock Reset
- Temp Monitor
- Smart DMA
- System Buses

Timers
- GPT
- Watchdog
- PWM x 2
- EPIT

Analog
- PLL x 3
- 24 MHz, 32 kHz Osc

Security
- RNG
- SRTC
- eFuses
- AES, SHA-1, SHA-2

System Debug
- Secure JTAG

Core/Internal Memory
- ARM® Cortex™-A8
- Cache
- ETM
- NEON™
- VFP
- ROM
- RAM

Multimedia
- GPU OpenVG™ 1.1
- EPDC Electronic Paper Display Controller Source/Gate Driver I/F
- ePxP
  - CSC
  - Combining
  - Rotation
  - Gamma Mapping
- eLCD I/F 8-, 16-, 24- and 32-bit DOTCK, RGB

Audio
- I²S/SSI/AC97 x 2

Standard Connectivity
- UART x 5
- eSDHC x 4
- I²C x 3
- KPP (8x8)
- eCSPI x 2
- CSPI

Advanced Connectivity
- USB OTG + PHY
- FEC 10/100
- USB Host + PHY

External Memory I/F
- 2 GB DDR2, mDDR, LP-DDR2

External Storage I/F
- RAW NAND
- SD/MMC
- 32-bit ECC
- PSRAM
- OneNAND
- NOR Flash

About the MC34708 PMIC

The Freescale MC34708 power management IC (PMIC) is optimized for use with the i.MX50 and helps maximize power efficiency and battery life while supporting higher levels of integration to minimize board space and cost. The MC34708 provides dual phase switchers for the i.MX50 core and memory, and it provides the USB/UART/audio switching for the mini/micro USB connector which reduces the connector count for a more compact design. A switching charger with dual inputs enables faster charging from a current limited source, such as USB and the dual path enables power on even when the battery has died. The MC34708 supports the universal charging standard to enable the selection of the optimal charging profile for the given charger source.

Freescale PMICs are exclusively designed to work with our i.MX processor family, providing optimized feature sets for specific applications.

Freescale's proven combined solutions are available as reference designs with full board support packages (BSPs) and backed by integrated technical support to offer quality solutions that get our customers to market faster.

Development Can Start Now

The Smart Application Blueprint for Rapid Engineering (SABRE) platform for eReaders based on i.MX50 is a new reference design available now. The SABRE platform for eReaders is based on the i.MX50 EVK and includes an E Ink EPD display board. For more information, visit **freescale.com/SABRE**.

For current information about Freescale products and documentation, please visit freescale.com/iMX50. Join fellow i.MX developers online at imxcommunity.org—an active community of open source developers.

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