

## General Description

The AOZ1401 is an integrated Li+ charger protection IC that protects against input over-voltage, input over-current, and battery over-voltage conditions. When the device detects an input over-voltage condition, it disconnects output from input by turning off the internal MOSFET switch, preventing damage of the charger. When the device detects a battery over-voltage condition, it also turns off the internal MOSFET to prevent battery from being over-charged. In the case of an over-current condition, it limits the input current at the current limit level set by an external resistor, and if the over-current persists, it turns off the internal MOSFET after a blanking period. The thermal shutdown feature adds another layer of protection.

The fault status indicator provides status information about fault conditions to the host.

The AOZ1401 is available in a 2mm x 2mm 8-pin DFN package and is rated over a -40°C to +85°C ambient temperature range.

## Features

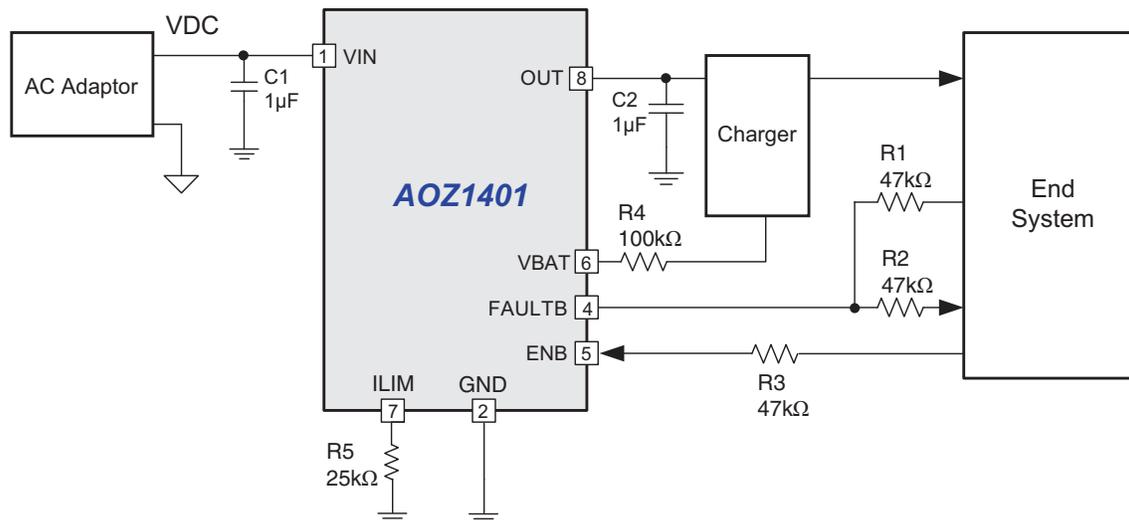
- Provides protection for three variables:
  - Input over-voltage
  - User-programmable input over-current
  - Battery over-voltage
- 30V maximum input voltage
- Supports up to 1.5A input current
- High immunity against false triggering due to voltage spikes
- Robust against false triggering due to current transients
- Thermal Shutdown
- Status indication, fault condition
- Available in space-saving small 8 lead 2x2 DFN

## Applications

- Smart Phones
- PDAs
- MP3 Players
- Low-Power handheld devices
- Bluetooth headsets



## Typical Application



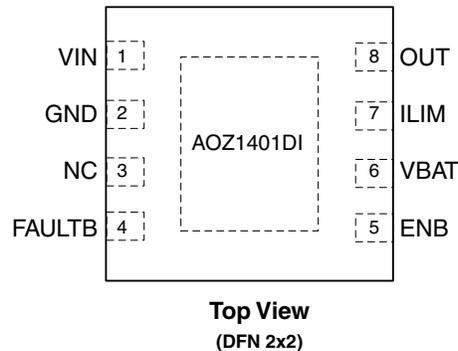
## Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1401DI	-40°C to +85°C	2 x 2 DFN-8	RoHS Compliant



All AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Parts marked as Green Products (with "L" suffix) use reduced levels of Halogens, and are also RoHS compliant. Please visit [www.aosmd.com/web/quality/rohs\\_compliant.jsp](http://www.aosmd.com/web/quality/rohs_compliant.jsp) for additional information.

## Pin Configuration



## Pin Description

Pin Name	Pin Number	I/O	Description
VIN	1	I	Input power, connect to external DC supply. Connect external 1 $\mu$ F (minimum) to GND
GND	2		Ground terminal
NC	3		These pins may have internal circuits used for test purposes. Do not make any external connections at these pins for normal operation.
FAULTB	4	O	Open-drain output, device status. FAULTB = LO indicates that the input FET has been turned off due to input over-voltage or input over-current conditions, or because the battery voltage is outside safe limits.
ENB	5	I	Chip enable input. Active low. When ENB = HI, the input FET is off. Internally pulled down.
VBAT	6	I	Battery voltage sense input. Connect to pack positive terminal through a resistor.
ILIM	7	I/O	Input over-current threshold programming. Connect a resistor to GND to set the over-current threshold.
OUT	8	O	Output terminal to the charging system. Connect external 1 $\mu$ F capacitor (minimum) to GND
Thermal PAD			There is an internal electrical connection between the exposed thermal pad and the GND pin of the device. The thermal pad must be connected to the same potential as the GND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. GND pin must be connected to ground at all times.

## Absolute Maximum Ratings<sup>(1)</sup>

Parameter	Pin Name	Rating
Input Voltage	VIN (with respect to GND)	-0.3V to 30V
Input Voltage	OUT(with respect to GND)	-0.3V to 12V
Input Voltage	ILIM, FAULTB, ENB, VBAT (with respect to GND)	-0.3V to 7V
Input Current	VIN	2.0A
Output Current	OUT	2.0A
Output Sink Current	FAULTB	15mA
Junction Temperature, T <sub>J</sub>		-40°C to 150°C
Storage Temperature, T <sub>STG</sub>		-65°C to 150°C
Lead Temperature (Soldering, 10 seconds)		300°C
ESD (Human Body Model)		2kV
ESD (Machine Model)		200V

### Note:

- Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

## Recommended Operating Conditions

Parameter	Conditions	Min.	Max.	Units
V <sub>VIN</sub>	VIN Voltage Range	3.3	26	V
I <sub>VIN</sub>	Input Current, VIN pin		1.5	A
I <sub>OUT</sub>	Current, OUT pin		1.5	A
R <sub>ILIM</sub>	OCP Programming Resistor	15	90	kΩ
T <sub>J</sub>	Junction Temperature	0	125	°C

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  and  $V_{IN} = 5\text{V}$ , unless otherwise stated. Specifications in **BOLD** are guaranteed by design for ambient temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
<b>VIN</b>						
$V_{UVLO}$	Under-Voltage Lock-out, Input Power Detected Threshold	ENB = LO	2.6	2.7	2.8	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	ENB = LO		260		mV
$T_{DGL(PGOOD)}$	Deglitch Time, Input Power Detected Status	ENB = LO		8		ms
$I_{DD}$	Operating Current	ENB = LO, No Load on OUT pin, $V_{IN} = 5.0\text{V}$ , $R_{ILIM} = 25\text{k}\Omega$		400	500	$\mu\text{A}$
$I_{STDBY}$	Standby Current	ENB = HI, $R_{ILIM} = 25\text{k}\Omega$		70	95	$\mu\text{A}$
<b>INPUT TO OUTPUT CHARACTERISTICS</b>						
$V_{DO}$	Drop-Out Voltage VIN to OUT	ENB = LO, $I_{OUT} = 1\text{A}$			300	mV
<b>INPUT OVER-VOLTAGE PROTECTION</b>						
$V_{OVP}$	Input Over-Voltage Protection Threshold	ENB = LO	<b>5.67</b>	<b>5.85</b>	<b>6.00</b>	V
$t_{PD(OVP)}$	Input OV Propagation Delay	ENB = LO			1	$\mu\text{s}$
$V_{HYS-OVP}$	Hysteresis on OVP	ENB = LO or HI		60		mV
$t_{ON(OVP)}$	Recovery Time from Input Over-voltage Condition	ENB = LO		8		ms
<b>INPUT OVER-CURRENT PROTECTION</b>						
	Input Over-Current Protection Threshold Range	ENB = LO	300		1500	mA
$I_{OCP}$	Input Over-Current Protection Threshold	ENB = LO, $R_{ILIM} = 25\text{k}\Omega$	930	1000	1070	mA
$K_{ILIM}$	Current Limit Programming: $I_{OCP} = K_{ILIM} / R_{ILIM}$			25		$\text{k}\Omega$
$t_{BLANK(OCP)}$	Blanking Time, Input Over-Current Detected	ENB = LO		176		$\mu\text{s}$
$t_{ON(OCP)}$	Recovery Time from Input Over-current Condition	ENB = LO		64		ms
<b>BATTERY OVER-RANGE PROTECTION</b>						
$BV_{OVP}$	Battery Over-Voltage Protection Threshold	ENB = LO, $V_{IN} > 4.4\text{V}$	<b>4.30</b>	<b>4.35</b>	<b>4.4</b>	V
$V_{HYS-BOVP}$	Hysteresis on $BV_{OVP}$	ENB = LO, $V_{IN} > 4.4\text{V}$		270		mV
$I_{VBAT}$	Input Bias Current on VBAT pin				20	nA
$T_{DGL(BOVP)}$	Deglitch Time, Battery Over-Voltage Detected	ENB = LO		176		$\mu\text{s}$
<b>THERMAL PROTECTION</b>						
$T_{J(OFF)}$	Thermal Shutdown Temperature			140		$^\circ\text{C}$

**Electrical Characteristics** (Continued)

$T_A = 25^\circ\text{C}$  and  $V_{IN} = 5\text{V}$ , unless otherwise stated. Specifications in **BOLD** are guaranteed by design for ambient temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$T_{J(OFF-HYS)}$	Thermal Shutdown Hysteresis			20		$^\circ\text{C}$
<b>LOGIC LEVELS ON ENB</b>						
$V_{IL}$	Logic LOW Input Voltage		0		0.4	V
$V_{IH}$	Logic HIGH Input Voltage		1.4			V
$I_{IL}$		ENB = 0V			1	$\mu\text{A}$
$I_{IH}$		ENB = 1.8V			15	$\mu\text{A}$
<b>LOGIC LEVELS ON FAULTB</b>						
$V_{OL}$	Output LOW Voltage	$I_{SINK} = 5\text{mA}$			0.2	V
$I_{HI-Z}$	Leakage Current	$V_{FAULTB} = 5\text{V}$			10	$\mu\text{A}$

**Functional Block Diagram**

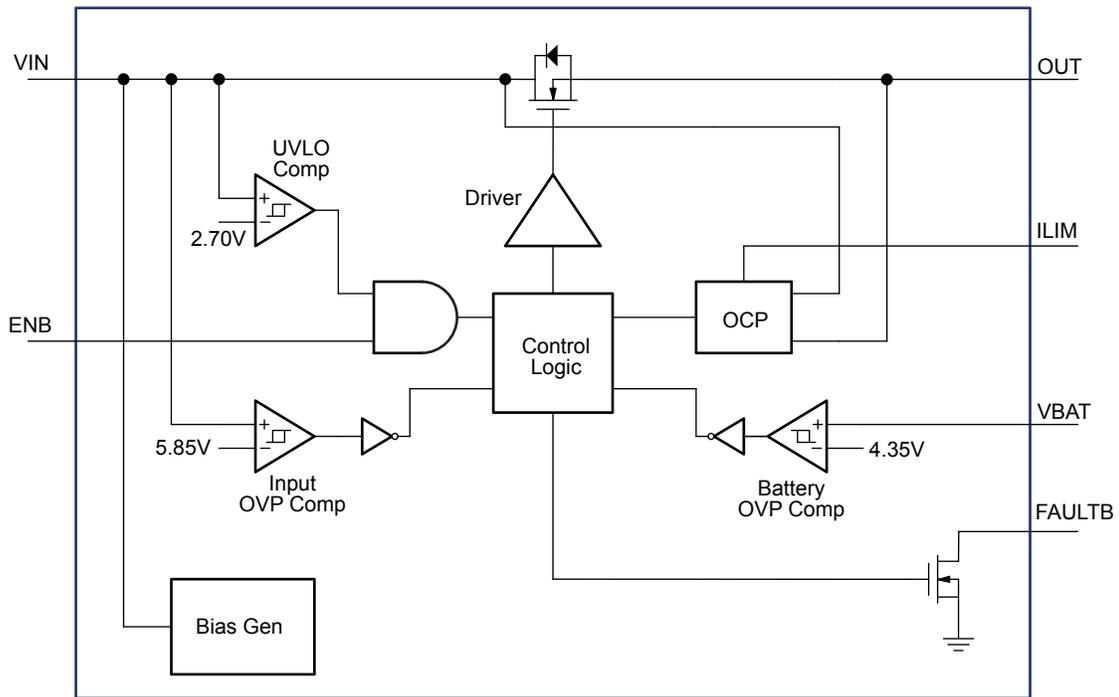


Figure 1. Simplified Block Diagram

## Functional Characteristics

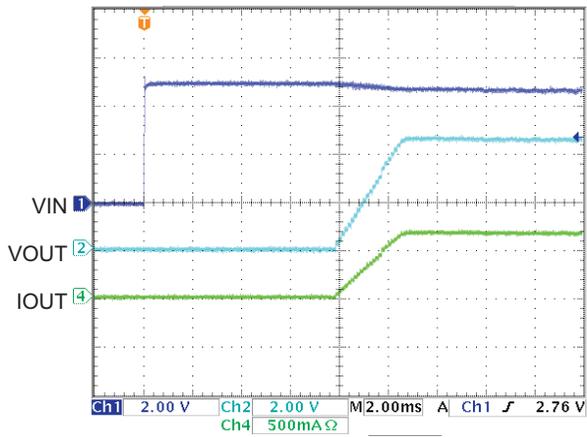


Figure 2. Normal Power-On Showing Soft-Start,  $R_{OUT} = 6.6\Omega$

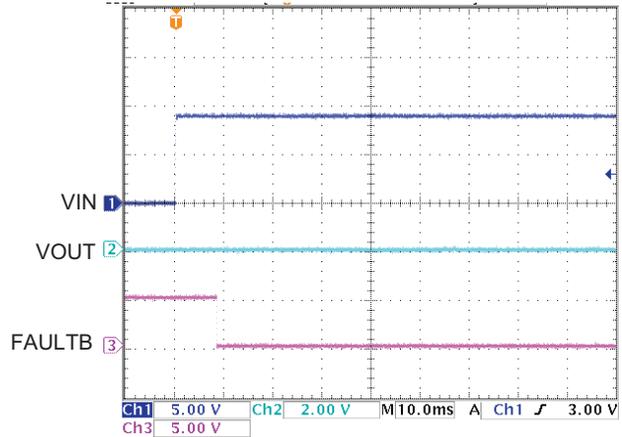


Figure 3. OVP at Power-On,  $V_{IN} = 0V$  to  $9V$

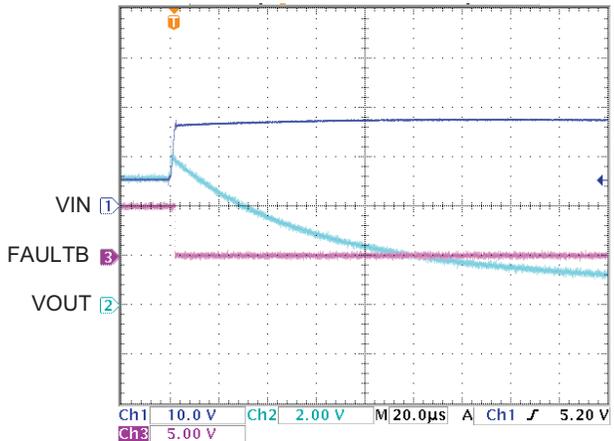


Figure 4. OVP Response for Input Step,  $V_{IN} = 5V$  to  $12V$ ,

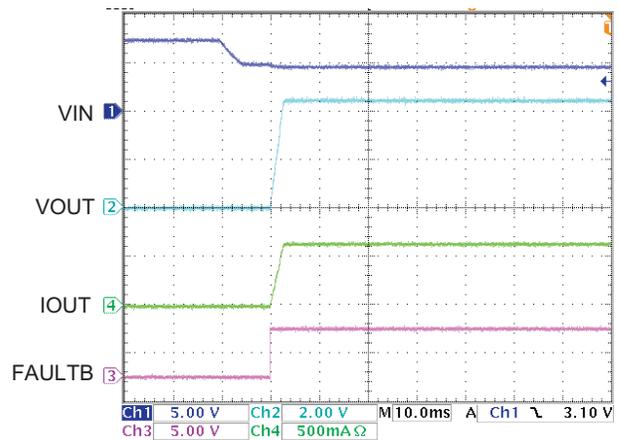


Figure 5. Recovery from OVP,  $V_{IN} = 7.5V$  to  $5V$

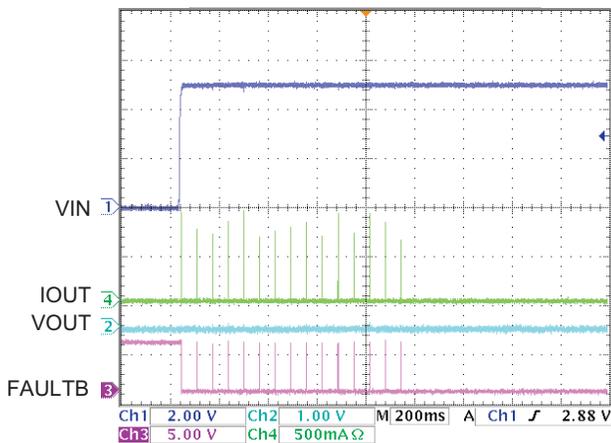


Figure 6. OCP, Powering Up into a Short Circuit on OUT Pin, OCP Counter Counts to 15 Before Switching OFF the Device

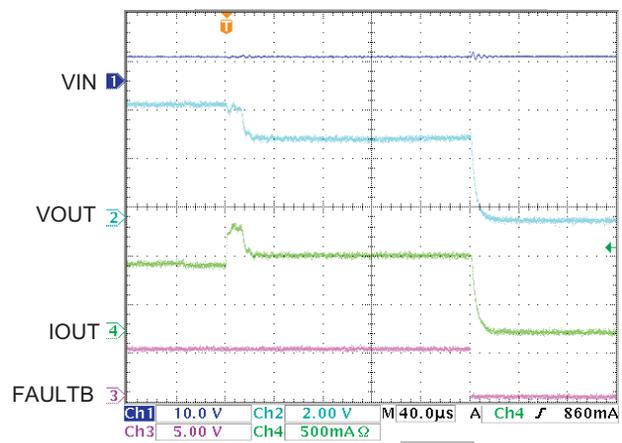


Figure 7. OCP,  $R_{OUT}$  Switches from  $6.6\Omega$  to  $3.3\Omega$ , Shows Current Limiting and Soft-stop

Functional Characteristics (Continued)

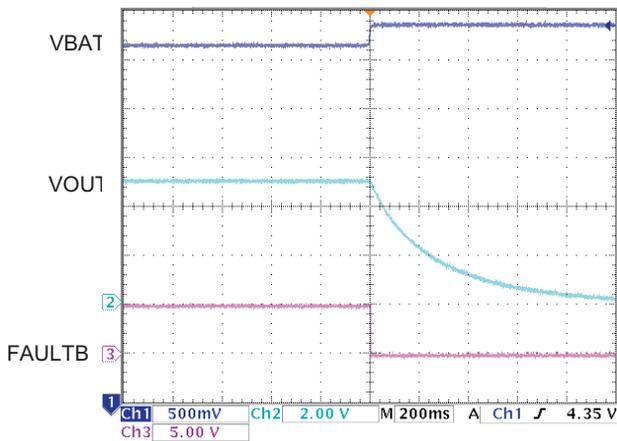


Figure 8. BAT-OVP,  $V_{VBAT}$  Steps from 4.2V to 4.4V

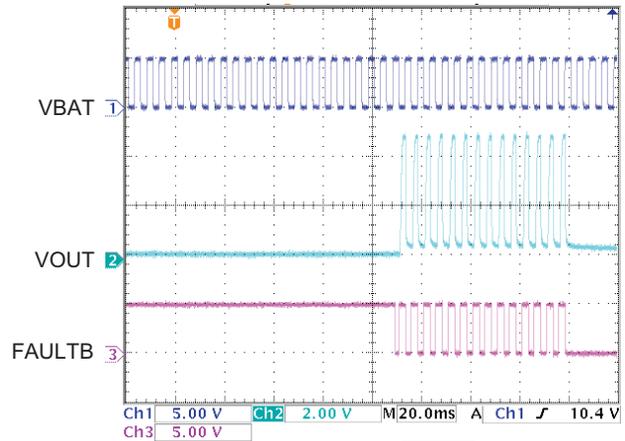


Figure 9. Battery OVP and Counter

Typical Operating Characteristics

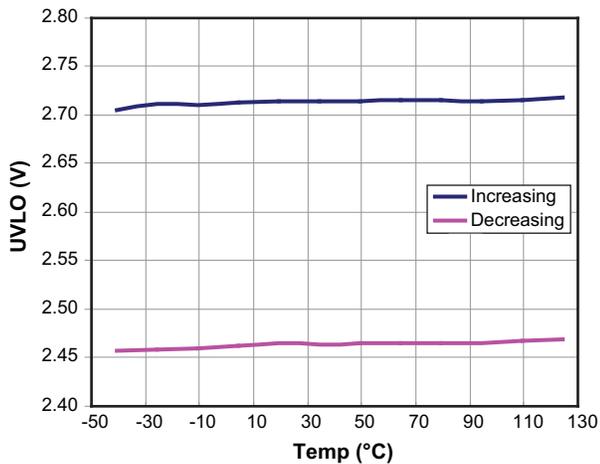


Figure 10. UVLO vs. Temperature

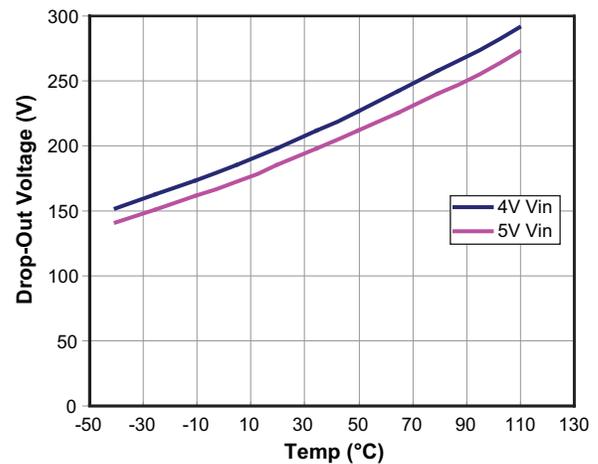


Figure 11. Drop-out Voltage vs. Temperature

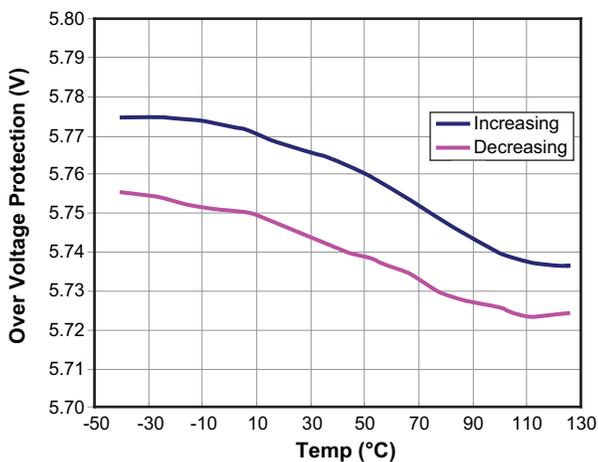


Figure 12. Over-voltage Protection vs. Temperature

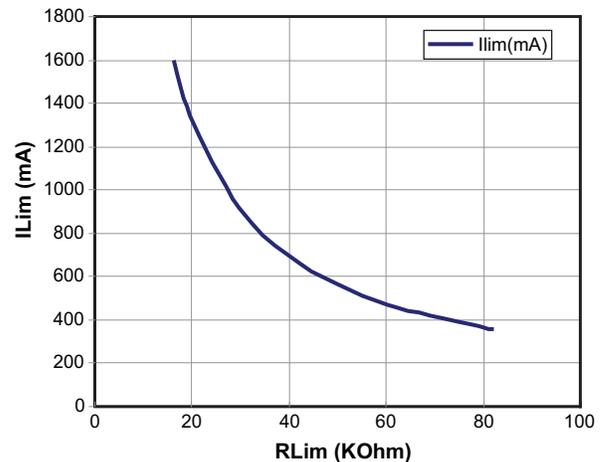


Figure 13. ILim vs. RLim

Typical Operating Characteristics (Continued)

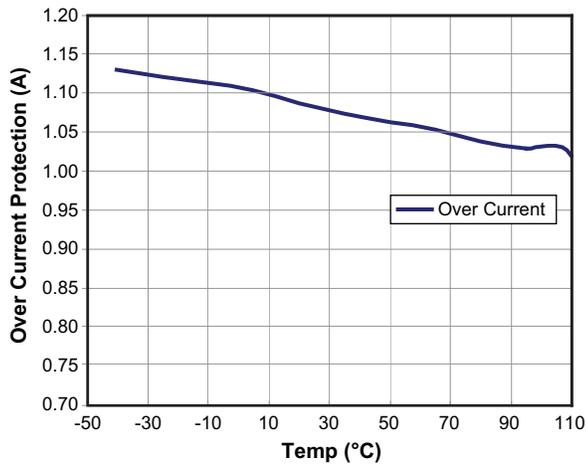


Figure 14. Over-current Protection vs. Temperature

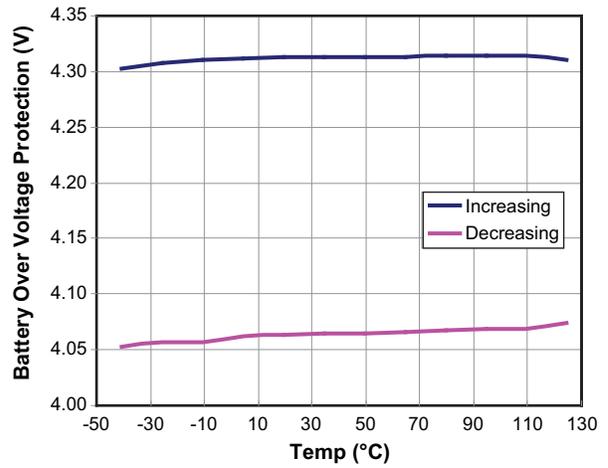


Figure 15. Battery Over Voltage Protection vs. Temperature

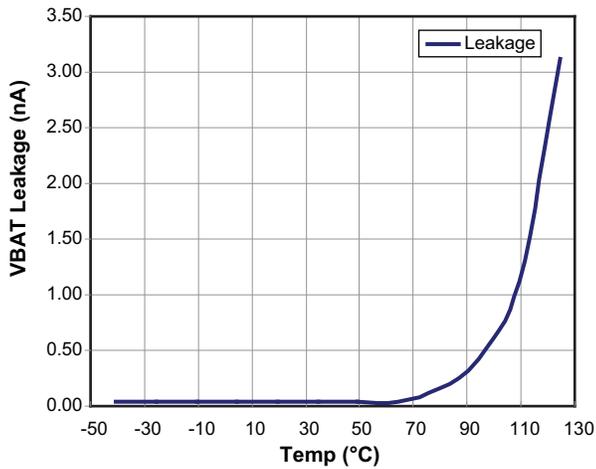


Figure 16. VBAT Leakage Current vs. Temperature

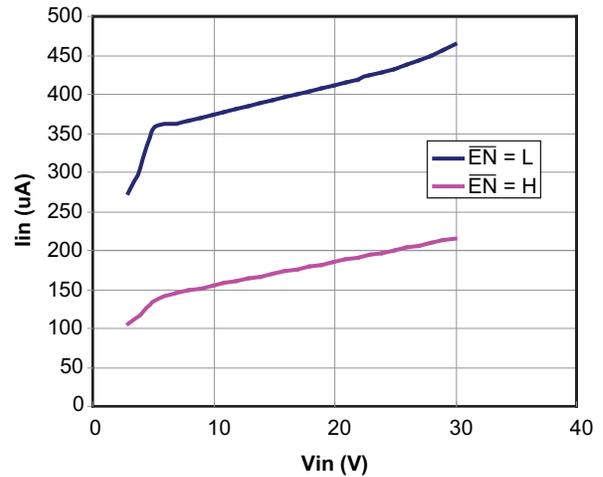
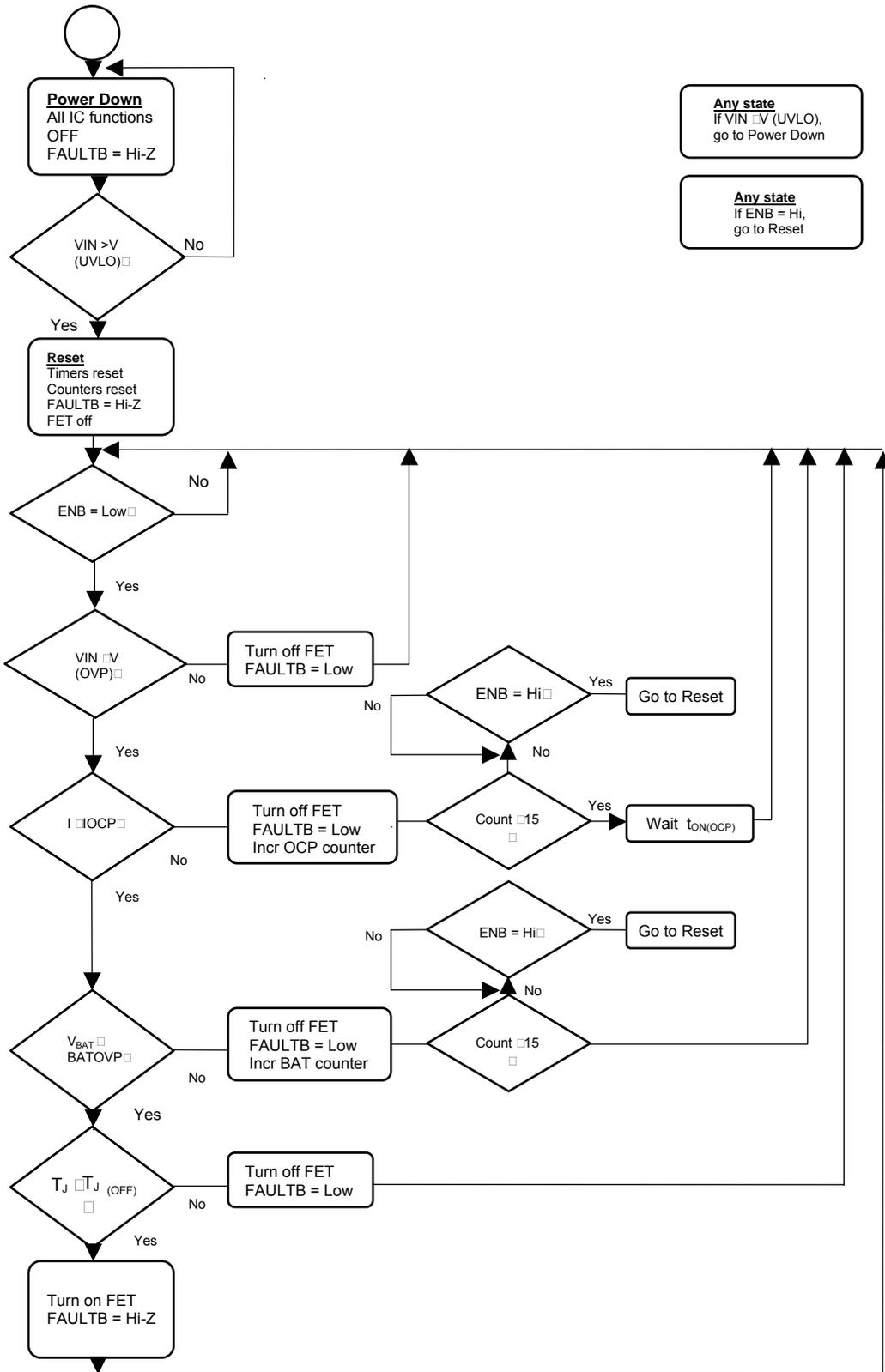


Figure 17. Supply Current vs. Input Voltage

Flow Chart



## Theory of Operation

The AOZ1401DI is an integrated Li+ charger protection IC that protects against input over-voltage, input over-current, and battery over-voltage conditions.

When the device detects an input over-voltage condition, it turns off the internal MOSFET, preventing damage of the charger.

When the device detects a battery over-voltage condition, it also turns off the internal MOSFET to prevent battery from being over-charged.

In the case of an over-current condition, it limits the input current at the current limit level set by an external resistor, and if the over-current persists, it turns off the internal MOSFET after a blanking period.

The thermal shutdown feature adds another layer of protection.

The fault status indicator provides status information about fault conditions to the host.

### Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit of AOZ1401DI monitors the input voltage and prevents the output MOSFET from turning on until  $V_{IN}$  exceeds 2.7V.

### Enable

The ENB pin is the ON/OFF control for the output switch. When the ENB pin is driven high, the internal FET is turned off. When the ENB pin is low, the FET is turned on.

### Input Overvoltage Protection

The device continuously monitors the input voltage, the input current, and the battery voltage. If the input voltage rises above  $V_{OVP}$ , the internal FET is turned off, removing power from the circuit. When the input voltage returns below  $V_{OVP}$ , but above  $V_{UVLO}$ , the FET is turned on again after a deglitch time of  $t_{ON(OVP)}$  to ensure that the input supply has stabilized.

### Input Overcurrent Protection

In the case of an over-current condition, AOZ1401DI limits the input current at the current limit level set by an external resistor, and if the over-current persists, it turns off the internal MOSFET after a blanking period. The overcurrent threshold is programmed by a resistor  $R_5$  ( $R_{ILIM}$ ) connected from the ILIM pin to VSS. Figure 13 shows the OCP threshold as a function of  $R_5$  ( $R_{ILIM}$ ), and may be approximated by the following equation:

$$I_{OCP} = 25 \div R_5 (R_{ILIM}) \text{ (current in A, resistance in k}\Omega\text{)}$$

### Battery Over-voltage Protection

The battery overvoltage threshold BVOVP is internally set to 4.35V. If the battery voltage exceeds the BVOVP threshold, the FET is turned off, and the FAULTB pin is driven low.

### FAULTB

The FAULTB pin is an open drain output that is asserted low when either an input overvoltage, input overcurrent battery overvoltage, or thermal overload condition occurs.

### Thermal Shut-down Protection

The thermal overload protection of AOZ1401DI is engaged to protect the device from damage should the die temperature exceeds safe margins due to a short circuit, extreme loading or heating from external sources.

## Application Information

### Input Capacitor Selection

Use a 1 $\mu$ F or larger capacitor for input bypassing. This will limit the input voltage drop during output transient conditions. 1 $\mu$ F capacitor should be adequate for most applications; however, higher capacitor values will further reduce the voltage drop. Place the bypass capacitor as close to the IN pins as feasibly possible.

### Output Capacitor Selection

Use a 1 $\mu$ F or larger capacitor between the OUT and GND pins. The capacitance does not affect the turn on slew rate; however, a larger capacitor will make the initial turn on transient smoother.

### Selection of $R_4$ ( $R_{VBAT}$ )

Direct-connecting battery to VBAT is not recommended. The voltage at the IN pin may appear on the VBAT pin if IC fails. Connecting the VBAT pin through  $R_4$  ( $R_{VBAT}$ ) prevents a large current from flowing into the battery in case of a failure of the IC, so choose  $R_4$  ( $R_{VBAT}$ ) value in the range 100k $\Omega$  to 470k $\Omega$ .

### Selection of $R_3$ ( $R_{EN}$ ), $R_2$ ( $R_{FAULTB}$ ), and $R_1$ ( $R_{PU}$ )

The ENB pin can be used to enable and disable the IC. ENB pin can be tied to ground or left un-connected, permanently enabling the device, if host is not presented. If host control is required, the ENB pin should be connected to the host through as large a resistor as possible.

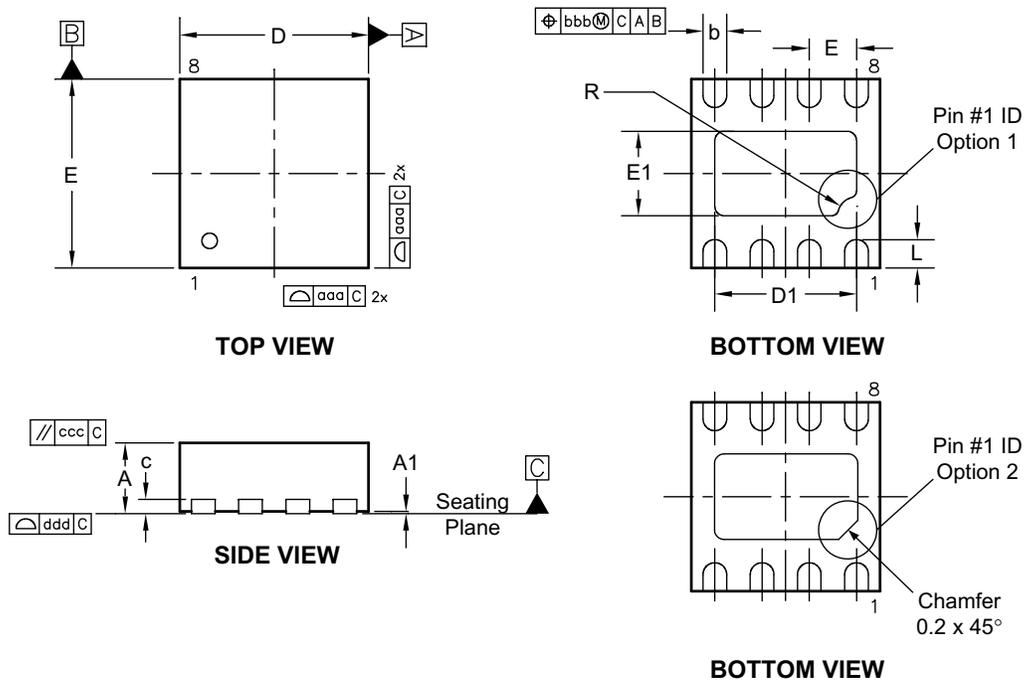
The FAULTB pin is an open drain output that is asserted low when either an input overvoltage, input overcurrent battery overvoltage, or thermal overload condition occurs. If the application does not require monitoring of

the FAULTB pin, it can be left unconnected. But if the FAULTB pin has to be monitored, it should be pulled high externally through  $R_1$  ( $R_{PU}$ ), and connected to the host through  $R_2$  ( $R_{FAULTB}$ ) prevents damage to the host controller if the AOZ1401DI fails. Choose the resistors with high values, and values between 22k $\Omega$  and 100k $\Omega$  should be sufficient.

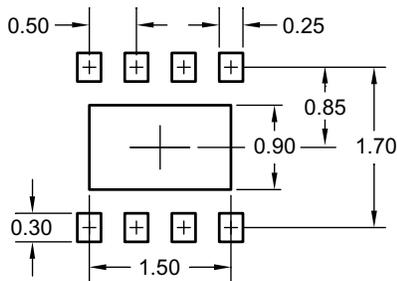
### **PCB Layout Guidelines**

AOZ1401DI uses DFN 2x2 package with a thermal PAD. The thermal PAD should be thermally coupled with the PCB ground plane for good thermal performance, This will require a copper pad directly under the IC in most applications. This copper pad should be connected to the ground plane with an array of thermal vias.  $C_{IN}$ ,  $C_{OUT}$ ,  $R_{LIM}$  and  $R_{BAT}$  should be located close to the IC.

Package Dimensions, DFN 2x2-8L



RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.20 REF.		
D	2.00 BSC		
D1	1.35	1.50	1.60
E	2.00 BSC		
E1	0.75	0.90	1.00
e	0.50 BSC		
L	0.20	0.30	0.40
R	0.20		
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.08		

Dimensions in inches

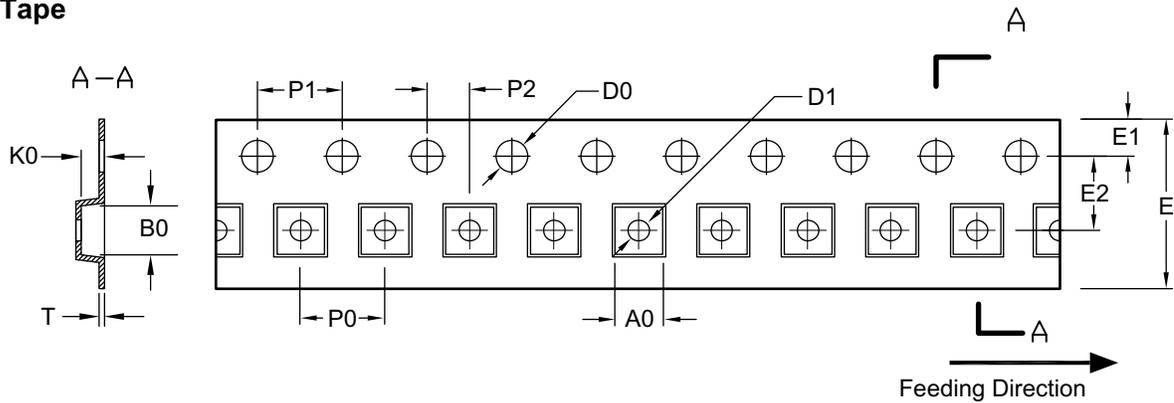
Symbols	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
b	0.007	0.010	0.012
c	0.008 REF.		
D	0.079 BSC		
D1	0.053	0.059	0.063
E	0.079 BSC		
E1	0.030	0.035	0.039
e	0.020 BSC		
L	0.008	0.012	0.016
R	0.008		
aaa	0.006		
bbb	0.004		
ccc	0.004		
ddd	0.003		

Notes:

1. Dimensions and tolerances conform to ASME Y14.5M-1994.
2. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
3. Dimension b applied to metallized terminal and is measured between 0.10mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, dimension b should not be measured in that radius area.
4. Coplanarity ddd applies to the terminals and all other bottom surface metallization.

## Tape and Reel Dimensions, DFN 2x2-8L

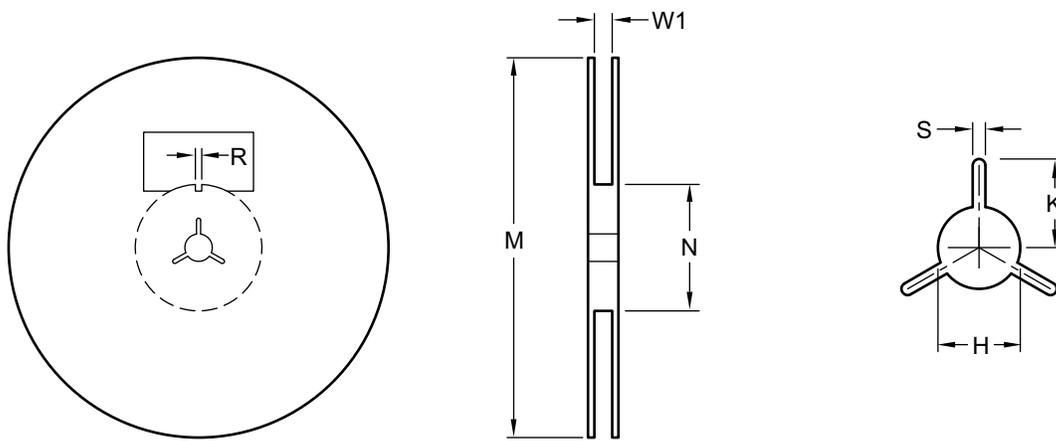
### Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 2x2	2.25 ±0.05	2.25 ±0.05	1.00 ±0.05	1.50 +0.10/-0	1.00 +0.25/-0	8.00 +0.30/-0.10	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.254 ±0.02

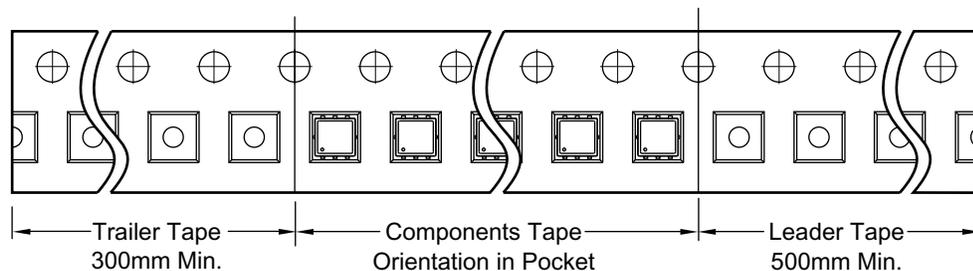
### Reel



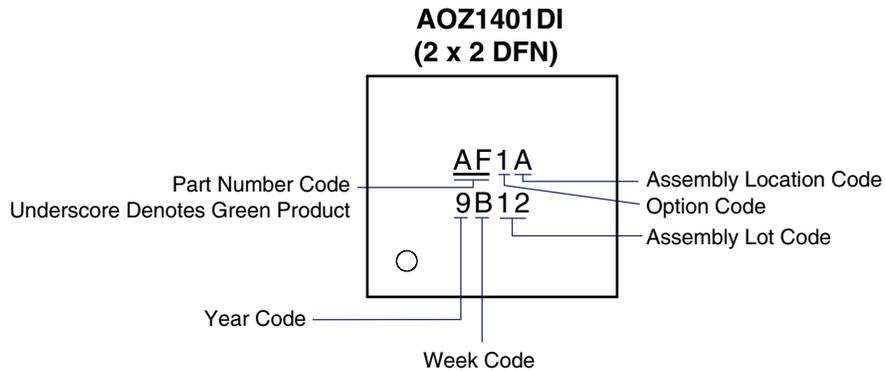
UNIT: mm

Tape Size	Reel Size	M	N	W1	H	S	K	R
8mm	ø180	ø180.00 ±0.50	60.0 ±0.50	8.4 +1.5/-0.0	13.0 ±0.20	1.5 Min.	13.5 Min.	3.0 ±0.50

### Leader / Trailer & Orientation



**Part Marking**



**This data sheet contains preliminary data; supplementary data may be published at a later date. Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.**

**LIFE SUPPORT POLICY**

ALPHA & OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.