

S4E5B001B000A00 Epson EPD Controller Module

Programming VCOM

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Chapter 1 VCOM Level Programming

This document describes how to program the VCOM level, which should match with the panel to be driven by the Epson EPD Controller Module, into the flash memory on the module.

1.1 Overview

Achieving high-quality images on an EPD requires the correct setting of the VCOM voltage. The common electrodes of all the pixels are connected together and a constant V_{common} voltage (VCOM) is required to drive these electrodes. The VCOM voltage should be set correctly on a panel-by-panel basis for best performance. Residual pixels (ghosting effect) will appear after display refresh if the VCOM voltage is not set correctly.

1.2 Recommended Programming Flow

The VCOM voltage is programmed as follows.

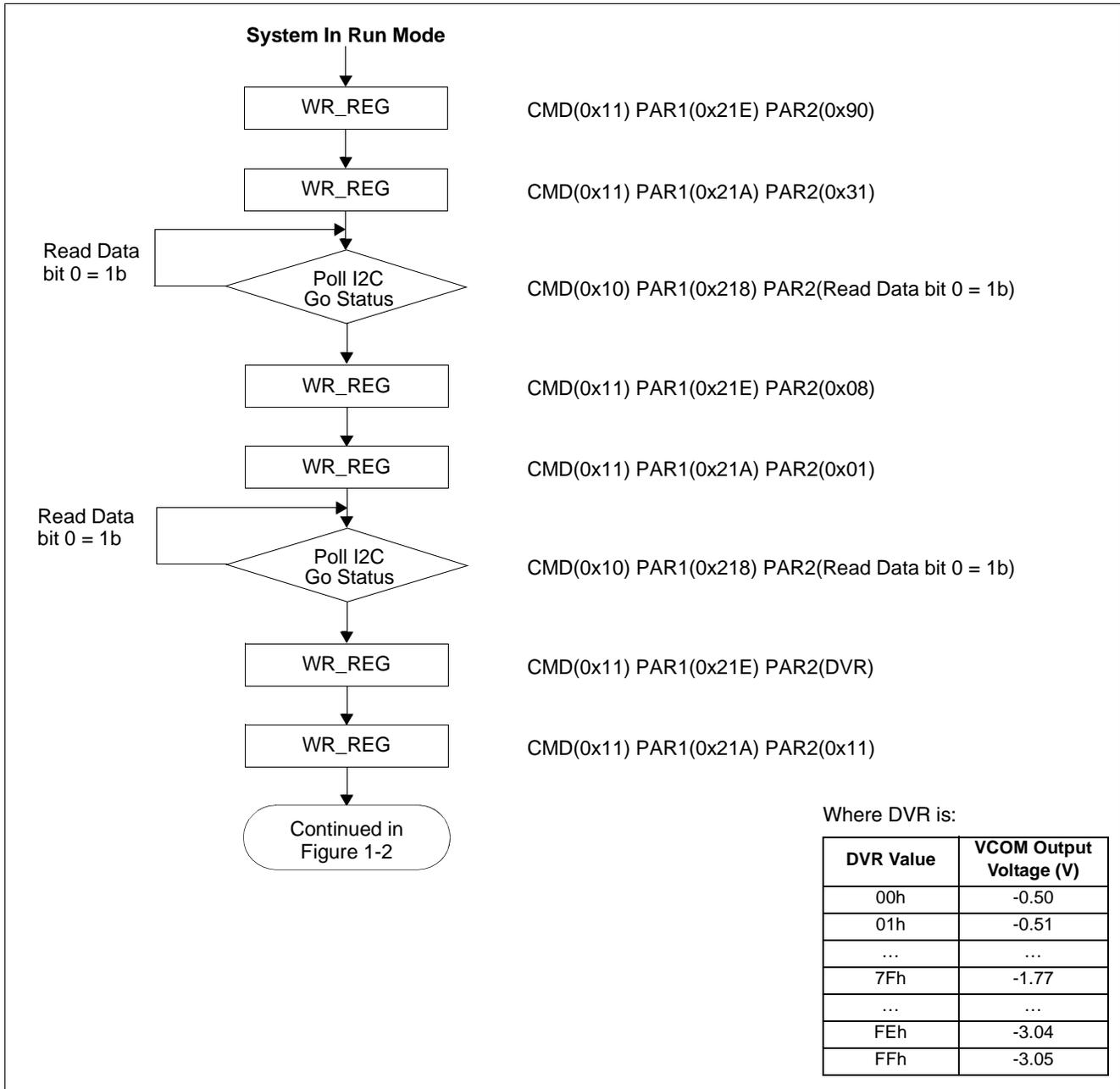


Figure 1-1: VCOM Programming Flow (1 of 2)

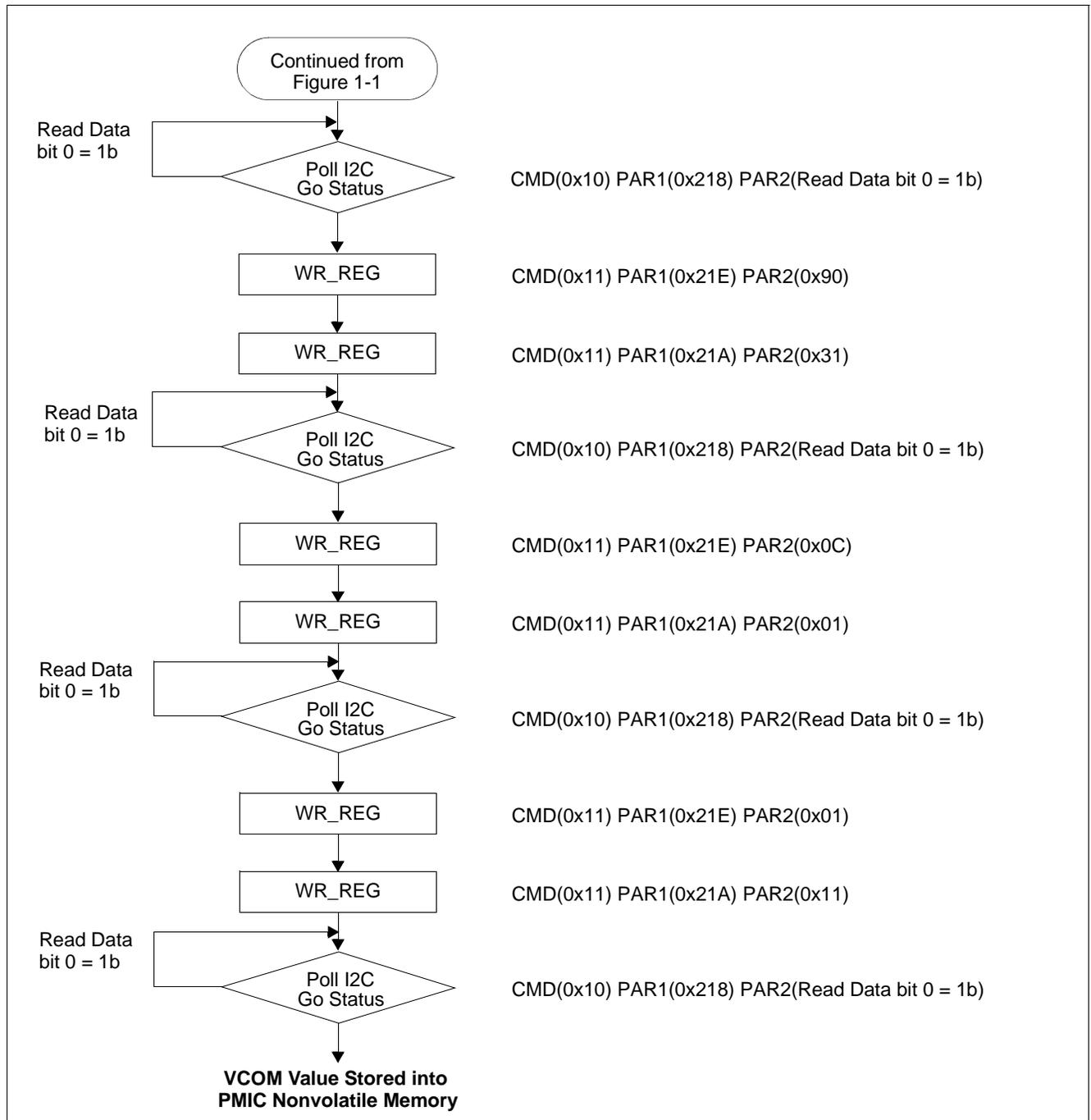


Figure 1-2: VCOM Programming Flow (2 of 2)

1.3 Reference Sample Code

```
// Defines for MAX17135
#define PMIC_DVR_REG                0x08
#define PMIC_PROG_CTRL_REG          0x0C

        :
        :

WORD epd_cmd_rd_reg(WORD index)
{
    // Platform-specific implementation of CMD(0x0010) PAR1(index)
    return PAR2;
}

void epd_cmd_wr_reg(WORD index, WORD value)
{
    // Platform-specific implementation of CMD(0x0011) PAR1(index) PAR2(value)
}

void epd_cmd_pmic_wr(BYTE index, BYTE value)
{
    epd_cmd_wr_reg(0x021E, 0x0090);
    epd_cmd_wr_reg(0x021A, 0x0031);
        while ((epd_cmd_rd_reg(0x0218)&0x0001) == 0x0001);
    epd_cmd_wr_reg(0x021E, (WORD) index);
    epd_cmd_wr_reg(0x021A, 0x0001);
        while ((epd_cmd_rd_reg(0x0218)&0x0001) == 0x0001);
    epd_cmd_wr_reg(0x021E, (WORD) value);
    epd_cmd_wr_reg(0x021A, 0x0011);
        while ((epd_cmd_rd_reg(0x0218)&0x0001) == 0x0001);
}

        :
        :

epd_cmd_pmic_wr(PMIC_DVR_REG, <DVR>); // Writing to PMIC DVR register
epd_cmd_pmic_wr(PMIC_PROG_CTRL_REG, 0x01); // Updating DVR register to PMIC nonvolatile memory

        :
        :
```

Change Record

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AMERICA

EPSON ELECTRONICS AMERICA, INC.

214 Devcon Drive
San Jose, CA 95112, USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH

Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.

7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-8522-1199 FAX: +86-10-8522-1125

SHANGHAI BRANCH

7F, Block B, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5577 FAX: +86-21-5423-4677

SHENZHEN BRANCH

12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.

Unit 715-723, 7/F Trade Square, 681 Cheung Sha Wan Road,
Kowloon, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346

EPSON TAIWAN TECHNOLOGY & TRADING LTD.

14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.

1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.**KOREA OFFICE**

5F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.**MICRODEVICES OPERATIONS DIVISION****IC Sales & Marketing Department**

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117