Power MOSFET

-60 V, -12 A, P-Channel DPAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low-voltage, highspeed switching applications in power supplies, converters, and power motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer an additional safety margin against unexpected voltage transients.

Features

- Avalanche Energy Specified
- I_{DSS} and V_{DS(on)} Specified at Elevated Temperature
- Designed for Low-Voltage, High-Speed Switching Applications and to Withstand High Energy in the Avalanche and Commutation Modes
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	-60	Vdc
Gate-to-Source Voltage - Continuous - Non-repetitive (t _p ≤ 10 ms)	V _{GS} V _{GSM}	± 20 ± 25	Vdc Vpk
Drain Current - Continuous @ T_a = 25°C - Single Pulse ($t_p \le 10$ ms)	I _D I _{DM}	-12 -18	Adc Apk
Total Power Dissipation @ T _a = 25°C	P_{D}	55	W
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 12 Apk, L = 3.0 mH, R_G = 25 Ω)	E _{AS}	216	mJ
Thermal Resistance - Junction-to-Case - Junction-to-Ambient (Note 1) - Junction-to-Ambient (Note 2)	$egin{array}{c} R_{ heta JC} \ R_{ heta JA} \ R_{ heta JA} \end{array}$	2.73 71.4 100	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 in. from case for 10 seconds	TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

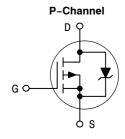
- 1. When surface mounted to an FR4 board using 1 in pad size (Cu area = 1.127 in^2).
- When surface mounted to an FR4 board using the minimum recommended pad size (Cu area = 0.412 in^2).



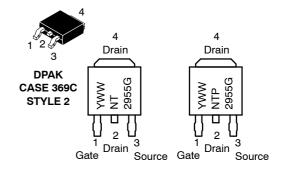
ON Semiconductor®

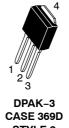
http://onsemi.com

V _{(BR)DSS} R _{DS(on)} TYP		I _D MAX
-60 V	155 mΩ @ –10 V, 6 A	-12 A

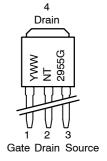


MARKING DIAGRAMS









Υ = Year WW = Work Week = Pb-Free Package

ORDERING INFORMATION

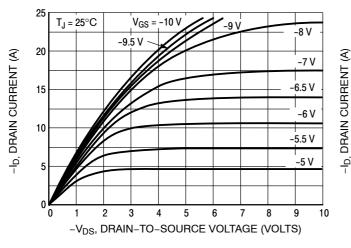
See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Cha	Symbol	Min	Тур	Max	Unit		
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Volta $(V_{GS} = 0 \text{ Vdc}, I_D = -0.25 \text{ mA})$ (Positive Temperature Coefficient	V _{(BR)DSS}	-60 -	_ 67	_ _	Vdc mV/°C		
Zero Gate Voltage Drain Current $(V_{GS} = 0 \text{ Vdc}, V_{DS} = -60 \text{ Vdc}, T_J = 25^{\circ}\text{C})$ $(V_{GS} = 0 \text{ Vdc}, V_{DS} = -60 \text{ Vdc}, T_J = 150^{\circ}\text{C})$		I _{DSS}	- -	- -	-10 -100	μAdc	
Gate-Body Leakage Current (V _{GS}	; = ± 20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	-100	nAdc	
ON CHARACTERISTICS (Note 3)		•					
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = -250 \mu Adc)$ (Negative Temperature Coefficients)	ent)	V _{GS(th)}	-2.0 -	-2.8 4.5	-4.0 -	Vdc mV/°C	
Static Drain-Source On-State Re (V _{GS} = -10 Vdc, I _D = -6.0 Adc)	R _{DS(on)}	-	0.155	0.180	Ω		
$\label{eq:controller} \begin{split} & \text{Drain-to-Source On-Voltage} \\ & \text{(V}_{GS} = -10 \text{ Vdc, I}_D = -12 \text{ Adc)} \\ & \text{(V}_{GS} = -10 \text{ Vdc, I}_D = -6.0 \text{ Adc,} \end{split}$	V _{DS(on)}		-1.86 -	-2.6 -2.0	Vdc		
Forward Transconductance (V _{DS} =	= 10 Vdc, I _D = 6.0 Adc)	gFS		8.0	-	Mhos	
DYNAMIC CHARACTERISTICS		'	1	•			
Input Capacitance		C _{iss}	-	500	750	pF	
Output Capacitance	(V _{DS} = -25 Vdc, V _{GS} = 0 Vdc, F = 1.0 MHz)	C _{oss}	-	150	250		
Reverse Transfer Capacitance	,	C _{rss}	_	50	100		
SWITCHING CHARACTERISTICS	(Notes 3 and 4)						
Turn-On Delay Time		t _{d(on)}	-	10	20	ns	
Rise Time	(V _{DD} = -30 Vdc, I _D = -12 A,	t _r	-	45	85		
Turn-Off Delay Time	$V_{GS} = -10 \text{ V}, R_G = 9.1 \Omega$	t _{d(off)}	-	26	40		
Fall Time		t _f	-	48	90		
Gate Charge		Q _T	-	15	30	nC	
	$(V_{DS} = -48 \text{ Vdc}, V_{GS} = -10 \text{ Vdc}, I_{D} = -12 \text{ A})$	Q _{GS}	-	4.0	-		
	,	Q_{GD}	-	7.0	_		
DRAIN-SOURCE DIODE CHARA	CTERISTICS (Note 3)						
Diode Forward On–Voltage $(I_S = 12 \text{ Adc}, V_{GS} = 0 \text{ V})$ $(I_S = 12 \text{ Adc}, V_{GS} = 0 \text{ V}, T_J = 150^{\circ}\text{C})$		V _{SD}	_ _	-1.6 -1.3	-2.5 -	Vdc	
Reverse Recovery Time		t _{rr}	-	50		ns	
$(I_S = 12 \text{ A}, dI_S/dt = 100 \text{ A}/\mu\text{s}, V_C$	as = 0 V)	ta	-	40	-	1	
		t _b	-	10	-		
Reverse Recovery Stored Charge		Q _{RR}	-	0.10	-	μС	

Indicates Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperature.

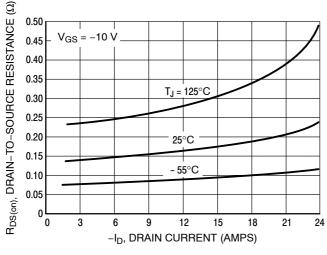
TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)



24 T_{J.}= - 55°C 22 $V_{DS} \ge -10 \text{ V}$. 125°C 20 18 16 14 12 10 0 3 8 9 10 -V_{GS}, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



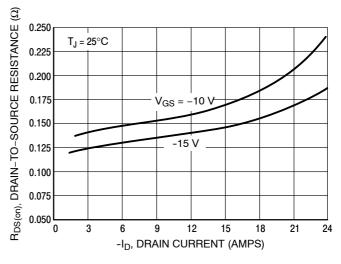
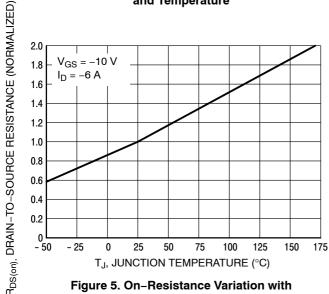


Figure 3. On-Resistance versus Drain Current and Temperature

Figure 4. On-Resistance versus Drain Current and Gate Voltage



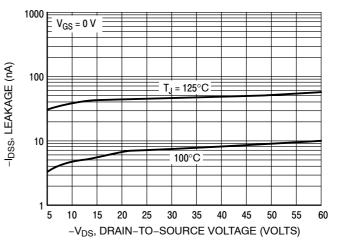
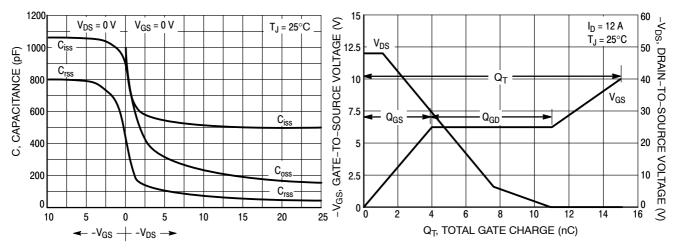


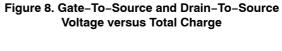
Figure 5. On-Resistance Variation with **Temperature**

Figure 6. Drain-To-Source Leakage **Current versus Voltage**



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (V)

Figure 7. Capacitance Variation



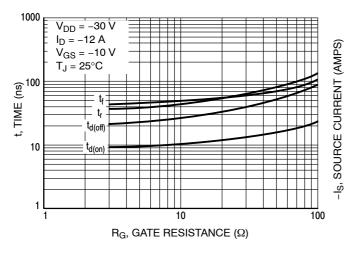


Figure 9. Resistive Switching Time Variation versus Gate Resistance

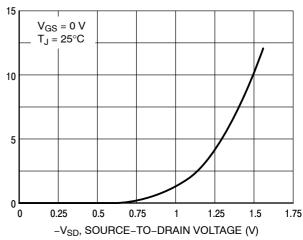


Figure 10. Diode Forward Voltage versus Current

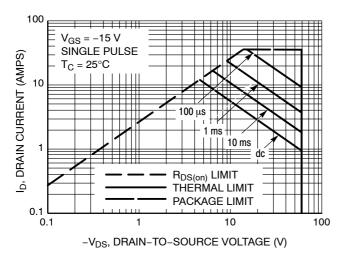


Figure 11. Maximum Rated Forward Biased Safe Operating Area

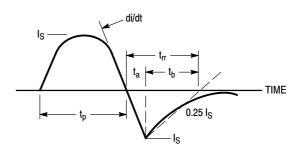


Figure 12. Diode Reverse Recovery Waveform

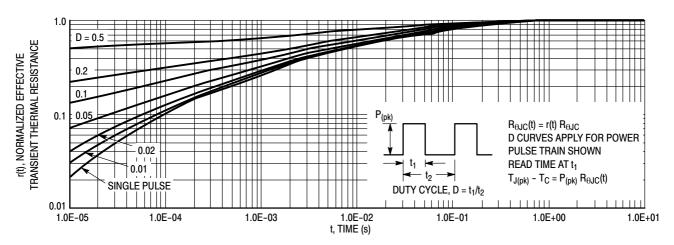


Figure 13. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD2955G	DPAK (Pb-Free)	75 Units / Rail
NTD2955-1G	IPAK (Pb-Free)	75 Units / Rail
NTD2955T4G	DPAK (Pb-Free)	
NTD2955PT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD2955T4G*	DPAK (Pb-Free)	

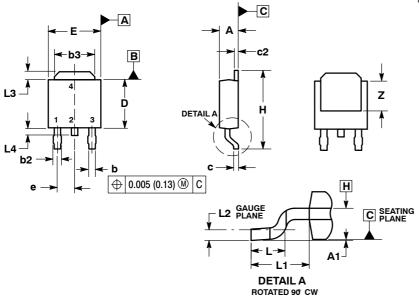
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP

Capable.

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)

CASE 369C ISSUE D



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: INCHES.

 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- MENSIONS b3, L3 and Z.

 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.

 5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

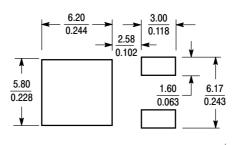
 6. DATUMS A AND B ARE DETERMINED AT DATUM

DATUMS A AND	BARE	DETERMINED	ΑT
PLANE H			

	INCHES MILLIMETER		IETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
b	0.025	0.035	0.63	0.89	
b2	0.030	0.045	0.76	1.14	
b3	0.180	0.215	4.57	5.46	
С	0.018	0.024	0.46	0.61	
c2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
Е	0.250	0.265	6.35	6.73	
е	0.090 BSC		2.29	.29 BSC	
Н	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.108 REF 2.74 R		REF		
L2	0.020	BSC	0.51 BSC		
L3	0.035	0.050	0.89	1.27	
L4		0.040		1.01	
Z	0.155		3.93		

STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

SOLDERING FOOTPRINT*

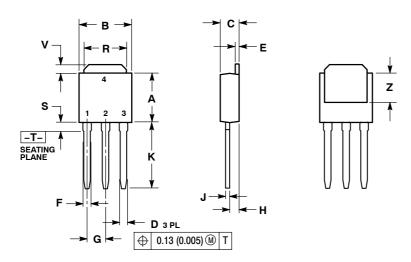


 $\left(\frac{\text{mm}}{\text{inches}}\right)$ SCALE 3:1

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

IPAK CASE 369D ISSUE C



NOTES:

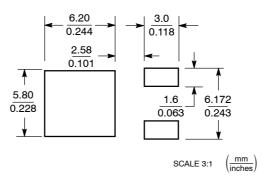
- 1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.

	INCHES MILLIMETER		IETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

STYLE 2: PIN 1. GATE

- 2. DRAIN
- 2. DRAIN 3. SOURCE
- 4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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