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EFM32LG840 Errata, Chip Rev. E

F256/F128/F64

This document describes errata for the latest revision of EFM32LG840 devices.

ARM ZERO TINY GECKO LEOPARD GIANT WONDER

SILICON LABS

1 Errata

This document contains information on the errata of the latest revision of this device. For errata on older revisions, please refer to the errata history for the device. The device data sheet explains how to identify chip revisions, either from package markings or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p1 (www.arm.com) also applies to this device.

1.1 Chip revision E

Table 1.1. Erratas

ID	Title/Problem	Effect	Fix/Workaround
BU_E105	**LFXO missing cycles during IOVDD ramping** LFXO missing cycles during IOVDD ramping when used in combination with Backup mode.	When IOVDD is ramped, the dc-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock.	Set PRESC in BURTC_CTRL to greater then 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock.
CMU_E114	**Device not waking up from EM2 when using prescaled non-HFRCO oscillator as HFCLK**	If the device is running from any prescaled oscillator other than HFRCO as HFCLK and HFRCO is disabled, the device will not wake up from EM2.	Before entering EM2, clear CMU_CTRL_HFCLKDIV. Alternatively, enable HFRCO by setting CMU_OSCENCMD_HFRCOEN and wait until CMU_STATUS_HFRCORDY is set.
DAC_E109	**DAC output drift over lifetime** The voltage output of the DAC might drift over time.	When the device is powered and the DAC is disabled, stress on an internal circuit node can cause the output voltage of the DAC to drift over time, and in some cases may violate the $V_{DACOFFSET}$ specification. If the DAC is always enabled while the device is powered, this condition cannot occur.	Both in the startup initialization code and prior to disabling the DAC in application code, set the OPAnSHORT bit in DACn_OPACTRL to a '1' for the corresponding DAC(s) used by the application. This will prevent the output voltage drift over time effect.
EMU_E107	**Interrupts during EM2 entry** An interrupt from a peripheral running from the high frequency clock that is received during EM2 entry will cause the EMU to ignore the SLEEPDEEP-flag.	During EM2 entry, the high frequency clocks that are disabled during EM2 will run for some clock cycles after WFI is issued to allow safe shutdown of the peripherals. If an enabled interrupt is requested from one of these non-EM2 peripherals during this shutdown period, the attempt to enter EM2 will fail, and the device will enter EM1 instead. As a result the pending interrupt will immediately wake the device to EM0.	Before entering EM2, disable all high frequency peripheral interrupts in the core.
PCNT_E102	**PCNT Pulse Width Filtering does not work**	The PCNT Pulse Width Filter does not work as intended.	Do not use the pulse width filter, i.e. ensure FILT = 0 in PCNTn_CTRL.

ID	Title/Problem	Effect	Fix/Workaround
TIMER_E103	**Capture/compare output is unreliable with RSSCOIST enabled** The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled.	When RSSCOIST is set and PRESC > 0 in TIMERn_CTRL, the capture/compare output value is not reliable.	Do not use a prescaled clock, i.e. ensure PRESC = 0 in TIMERn_CTRL when RSSCOIST is enabled.
RMU_E101	**POR calibration initialization issue** Upon initial power-on, some devices may not be able to access flash memory above the 4 kB boundary, or some calibration registers on some devices may not be set to their factory calibration values.	The list of affected devices can be found in the Knowledge Base (KB) article listed under Fix/Workaround. Some devices are sensitive to the power supply ramp during initial power-on. Specific ramp profiles on these devices can cause an intermittent issue resulting in one of two failure modes (A) or (B): A. Flash memory above the 4 kB boundary is inaccessible. Reads of the flash will return zeros. Write attempts will return an “invalid address” error code in the MSC_STATUS register. Code execution will behave as though the memory above 4 kB was filled with zeros until the device resets itself. B. Some parts of the calibration initialization process do not complete successfully. On USB devices, the USB voltage regulator does not get calibrated. Specific peripheral registers that may not be calibrated are as follows (not all registers apply to all devices): ADC0_CAL, IDAC_CAL, DAC0_CAL, DAC0_BIASPROG, DAC0_OPACTRL, and DAC0_OPAOFFSET. A SYSRESETREQ reset will clear either failure mode, and the device will behave normally until the next power-on event.	Additional information including a software workaround is available from the following KB article URL: http://community.silabs.com/t5/32-bit-MCU-Knowledge-Base/POR-calibration-initialization-issue/ta-p/154716

1.2 Older Revisions

Erratas for older revisions can be found at the Silicon Laboratories homepage:

www.silabs.com/32bit-errata

2 Revision History

2.1 Revision 1.10

October 5th, 2015

Added TIMER_E103.

Added PCNT_E102.

Added RMU_E101.

Added DAC_E109.

Added EMU_E107.

2.2 Revision 0.70

June 13th, 2014

Updated to product revision E.

Removed erratas that are not applicable to revision E.

2.3 Revision 0.60

August 21st, 2013

Added ADC_E117.

Added AES_E102.

Updated disclaimer, trademark and contact information.

2.4 Revision 0.50

July 30th, 2013

Added AES_E101.

Added BURTC_E102.

Added CMU_E114.

Added DMA_E101.

Updated errata naming convention.

2.5 Revision 0.40

June 5th, 2012

Added ADC1.

Added DI1.

2.6 Revision 0.30

April 24th, 2012

Added BU6.

Added CMU4.

Added CMU5.

Added LES3.

Added USART1.

Removed Erratas not valid for chip revision.

2.7 Revision 0.20

January 6th, 2012

Added CMU3.

Added CUR3.

Added CUR5.

Added MSC1.

Updated PRS1.

Removed Erratas not valid for chip revision.

2.8 Revision 0.10

November 4th, 2011

Initial preliminary release.

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