

# NTLJD4150P

## Power MOSFET

-30 V, -3.4 A,  $\mu$ Cool™ Dual P-Channel, 2x2 mm WDFN Package

### Features

- WDFN 2x2 mm Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- Footprint Same as SC-88 Package
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- Bidirectional Current Flow with Common Source Configuration
- This is a Pb-Free Device

### Applications

- Li-Ion Battery Charging and Protection Circuits
- LED Backlight, Flashlight
- Dual-High Side Load Switch

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	-30	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	-2.7	A
			$T_A = 85^\circ\text{C}$	-2.0	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$	$I_D$	-3.4	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	1.5	W
			$t \leq 5$ s	$P_D$	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	-1.8	A
		$T_A = 85^\circ\text{C}$	$I_D$	-1.4	
Power Dissipation (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	0.7	W
Pulsed Drain Current	$t_p = 10$ $\mu$ s	$I_{DM}$	-14	A	
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode) (Note 2)		$I_S$	-1.8	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

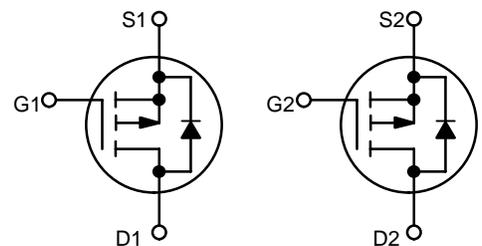
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size.



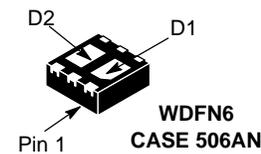
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$V_{(BR)DSS}$	$R_{DS(on)}$ Max	$I_D$ Max (Note 1)
-30 V	135 m $\Omega$ @ 10 V	-3.4 A
	200 m $\Omega$ @ 4.5 V	



P-CHANNEL MOSFET P-CHANNEL MOSFET



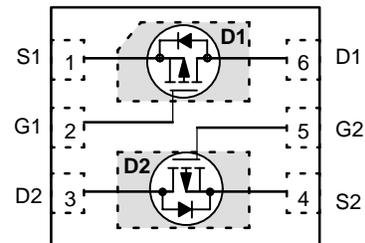
### MARKING DIAGRAM



- JE = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

Device	Package	Shipping†
NTLJD4150PTBG	WDFN6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

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## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
<b>SINGLE OPERATION (SELF-HEATED)</b>			
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	83	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	177	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	54	
<b>DUAL OPERATION (EQUALLY HEATED)</b>			
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	58	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 3)	$R_{\theta JA}$	133	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	40	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).  
 4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm<sup>2</sup>, 2 oz Cu).

## MOSFET ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ $\mu$ A	-30.0			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250$ $\mu$ A, Ref to $25^\circ\text{C}$		1.9		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -24$ V, $V_{GS} = 0$ V			-1.0	$\mu$ A
					-5.0	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			$\pm 100$	nA
<b>ON CHARACTERISTICS (Note 5)</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = -250$ $\mu$ A	-1.0	-1.5	-2.0	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			0.4		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -4.0$ A		95	135	m $\Omega$
		$V_{GS} = -4.5$ V, $I_D = -3.0$ A		156	200	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = -10$ V, $I_D = -1.0$ A		1.5		S

## CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = -15$ V		300		pF
Output Capacitance	$C_{OSS}$			50		
Reverse Transfer Capacitance	$C_{RSS}$			30		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5$ V, $V_{DS} = -15$ V, $I_D = -2.0$ A		3.6	4.5	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.44		
Gate-to-Source Charge	$Q_{GS}$			0.79		
Gate-to-Drain Charge	$Q_{GD}$			1.54		
Gate Resistance	$R_G$			10.6		$\Omega$

## SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5$ V, $V_{DD} = -24$ V, $I_D = -3.0$ A, $R_G = 2$ $\Omega$		7.0		ns
Rise Time	$t_r$			16.2		
Turn-Off Delay Time	$t_{d(OFF)}$			11.8		
Fall Time	$t_f$			8.8		

5. Pulse Test: Pulse Width  $\leq 300$   $\mu$ s, Duty Cycle  $\leq 2\%$ .  
 6. Switching characteristics are independent of operating junction temperatures.

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## MOSFET ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>							
Forward Recovery Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = -2.0\text{ A}$	$T_J = 25^\circ\text{C}$		-0.85	-1.0	V
			$T_J = 85^\circ\text{C}$		-0.77		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, d_{ISD}/d_t = 100\text{ A}/\mu\text{s},$ $I_S = -2.0\text{ A}$			8.9		ns
Charge Time	$t_a$				6.2		
Discharge Time	$t_b$				2.9		
Reverse Recovery Time	$Q_{RR}$				3.0		

5. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

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## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

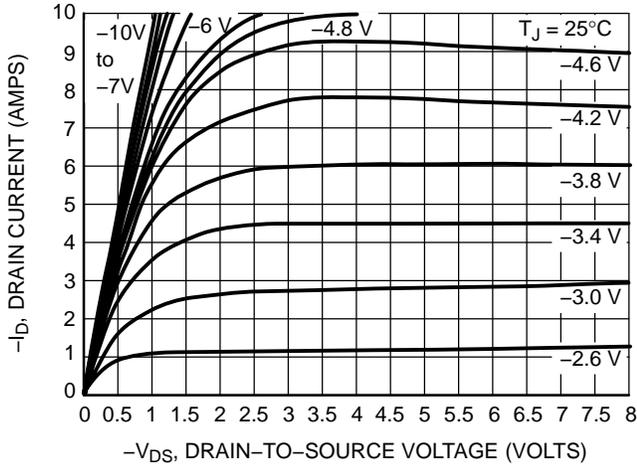


Figure 1. On-Region Characteristics

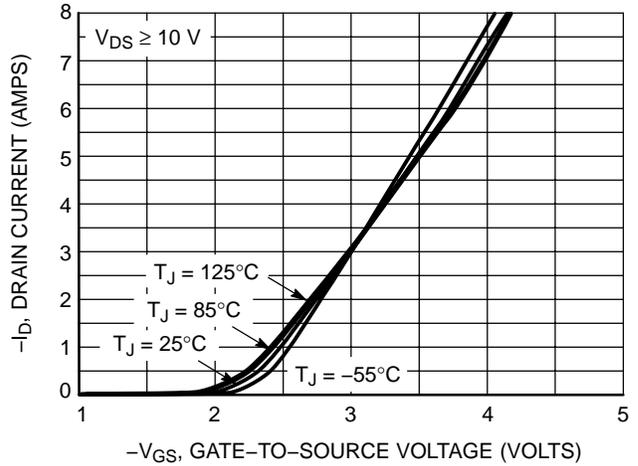


Figure 2. Transfer Characteristics

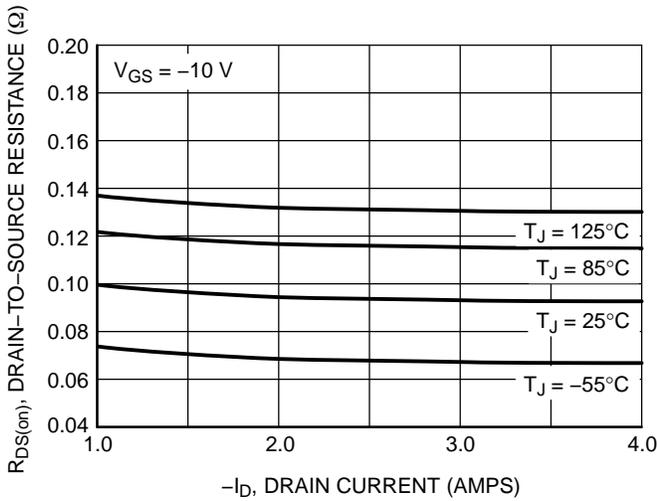


Figure 3. On-Resistance versus Drain Current

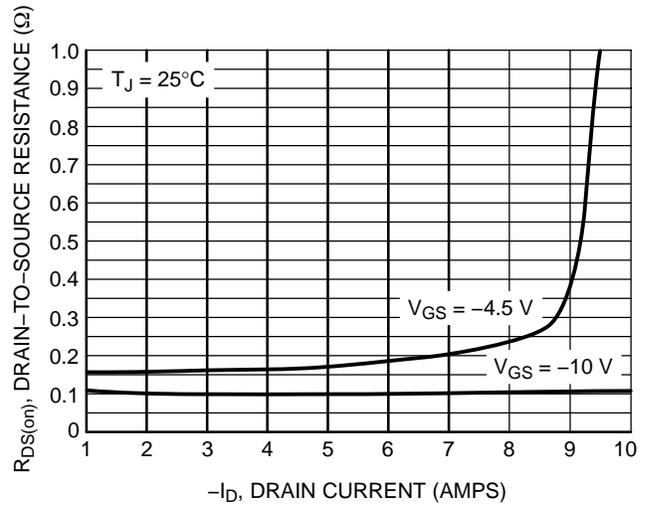


Figure 4. On-Resistance versus Drain Current and Gate Voltage

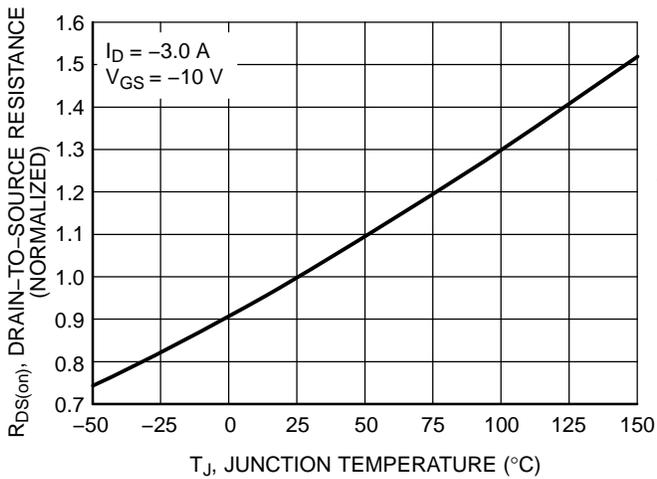


Figure 5. On-Resistance Variation with Temperature

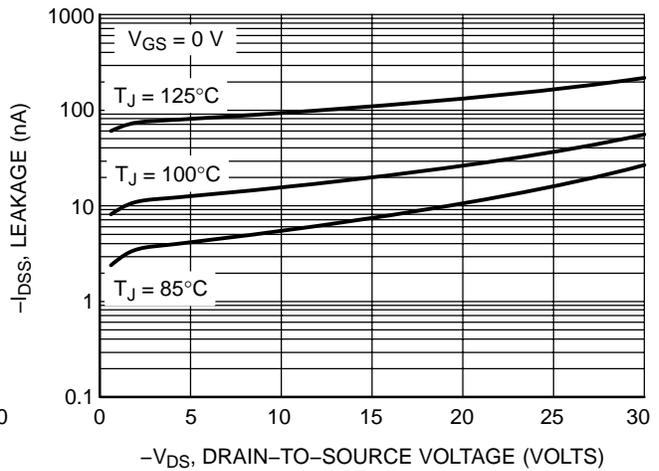


Figure 6. Drain-to-Source Leakage Current versus Voltage

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## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

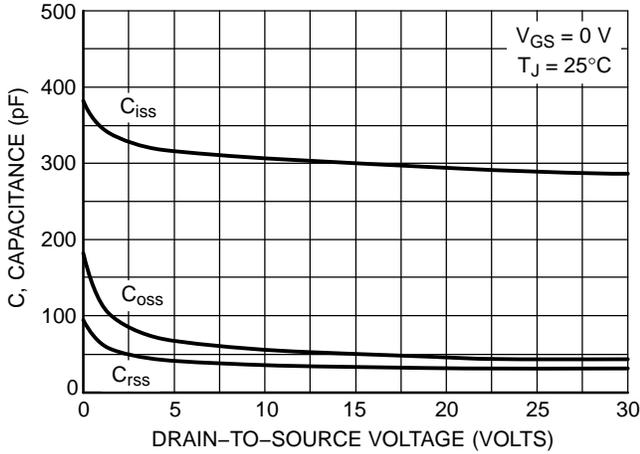


Figure 7. Capacitance Variation

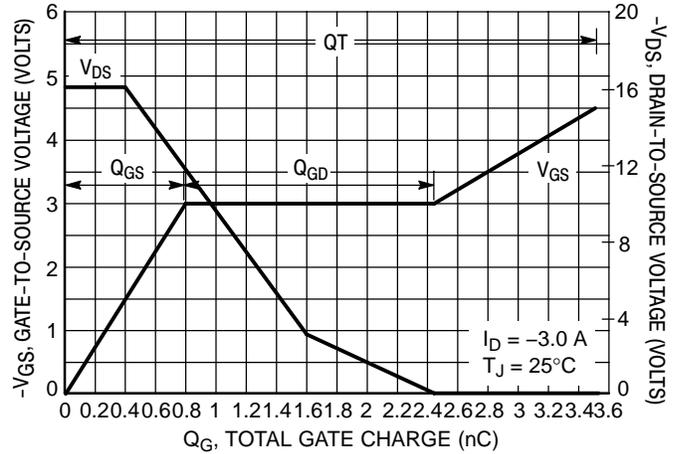


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

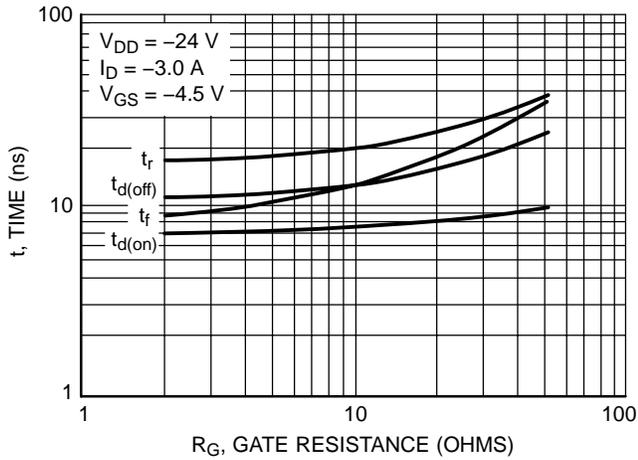


Figure 9. Resistive Switching Time Variation versus Gate Resistance

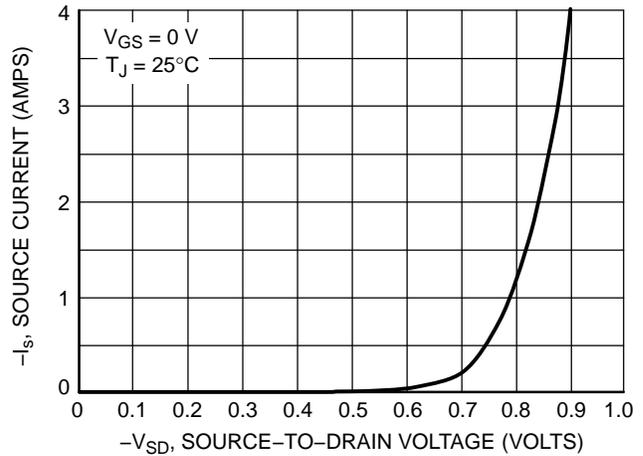


Figure 10. Diode Forward Voltage versus Current

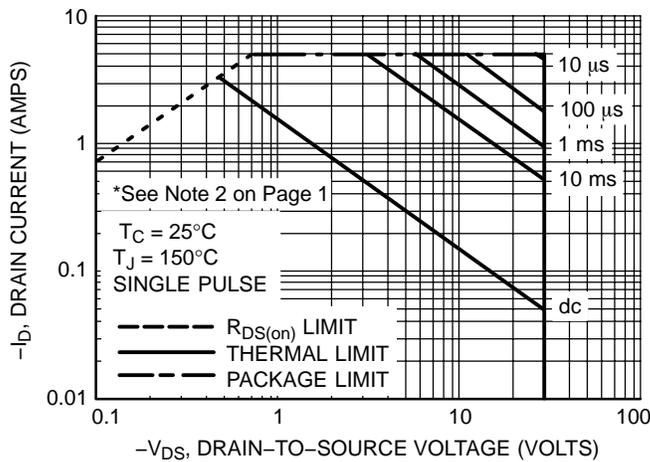


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

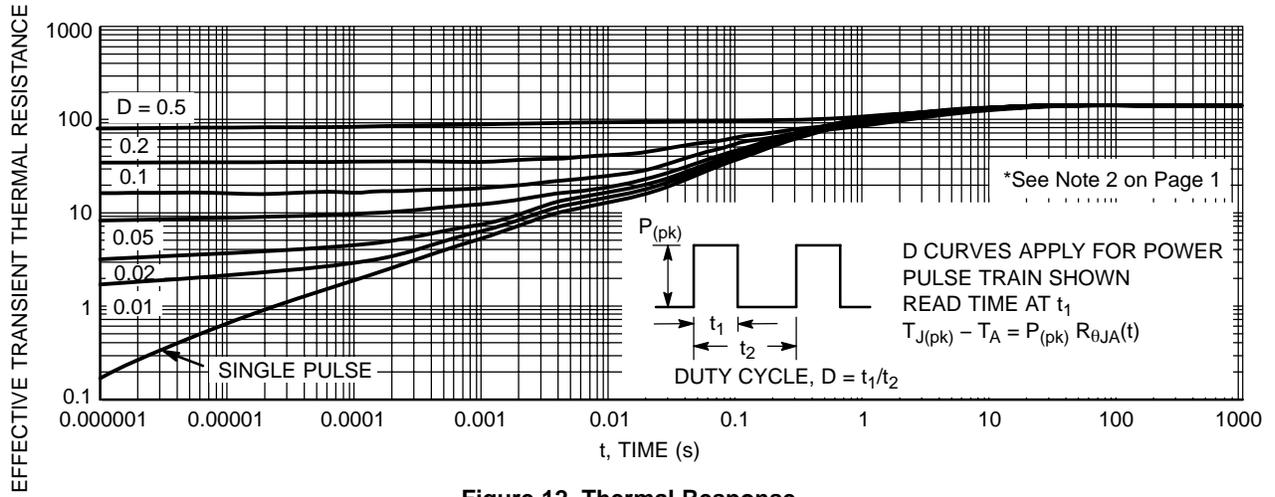
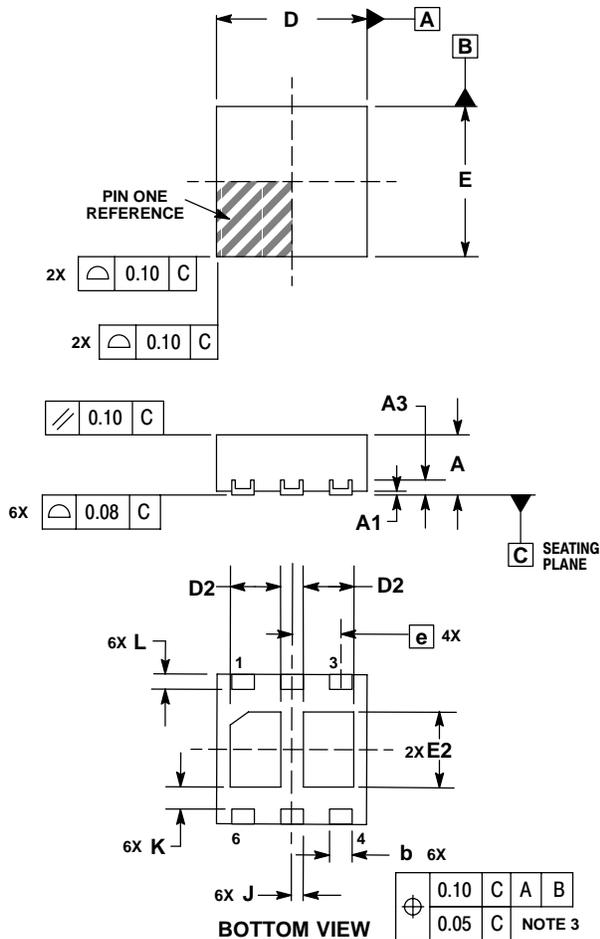


Figure 12. Thermal Response

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## PACKAGE DIMENSIONS

WDFN6 2x2  
CASE 506AN-01  
ISSUE C

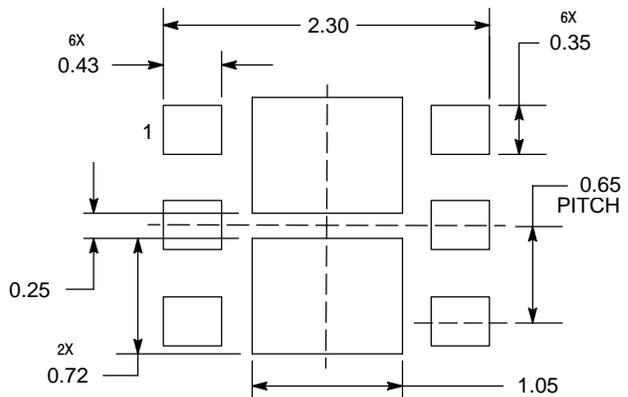


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
K	0.25 REF	
L	0.20	0.30
J	0.15 REF	

### SOLDERMASK DEFINED MOUNTING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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