PM8841

1 A low-side gate driver

Datasheet - production data

SOT23-5

Features

- Low-side MOSFET driver
- 1 A sink and 0.8 A source capability
- External reference for input threshold
- Wide supply voltage range (10 V ÷ 18 V)
- Input and output pull-down resistors
- Short propagation delays
- Input and output UVLO
- Wide operating temperature range: -40 °C to 125 °C
- SOT23-5 package

Applications

- SMPS
- Digital lighting
- Wireless battery chargers
- Digitally controlled MOSFETs

Description

The PM8841 is a high frequency single channel low-side MOSFET driver specifically designed to work with digital power conversion microcontrollers, such as the STMicroelectronics STLUX™ family of products.

The PM8841 output can sink 1 A and source 0.8 A.

The input levels of the driver are derived by the voltage present at the IN_TH pin (between 2 V and 5.5 V). This pin is typically connected at the same voltage of the microcontroller supply voltage.

The PM8841 device includes both input and output pull-down resistors.

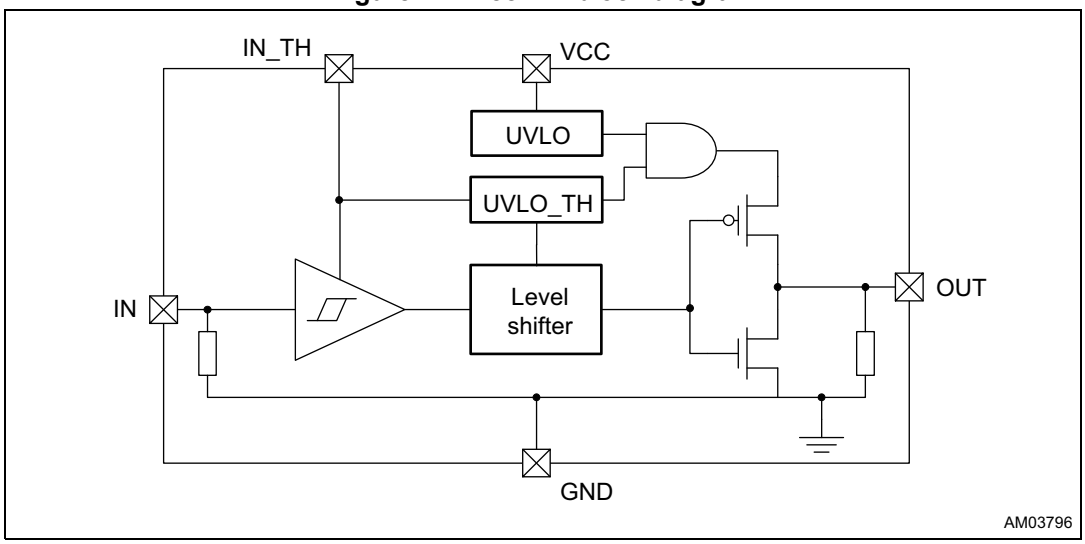
UVLO circuitry for input and output stages is present preventing the IC from driving the external MOSFET in unsafe condition.

Table 1. Device summary

Order code	Package
PM8841D	SOT23-5

1 Block diagram

Figure 1. PM8841D block diagram



2 Pin connection

Figure 2. Pin connection

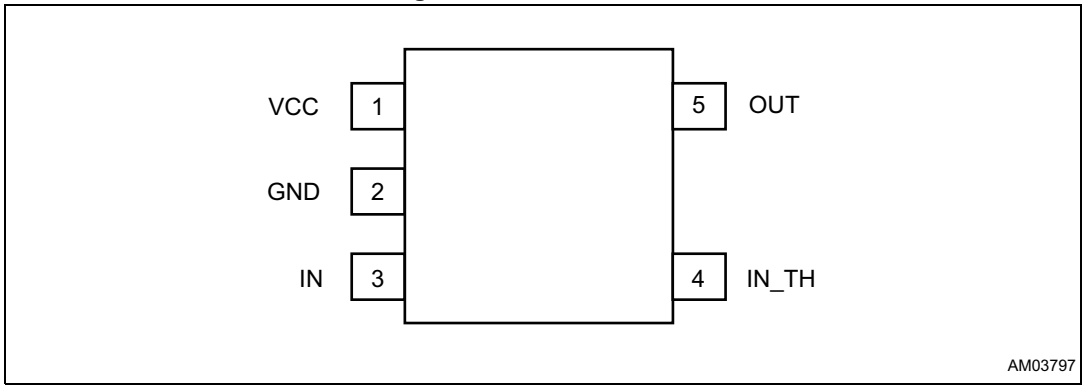


Table 2. Pin description

Symbol	Pin	Description
VCC	1	IC power supply. A voltage comprised between 10 V and 18 V can be connected between this pin and GND to supply the IC.
GND	2	Reference voltage connection.
IN	3	Digital input signal for driver. It is internally pulled down to GND with a 100 kΩ (typ.) equivalent resistor.
IN_TH	4	Input for the IN pin's threshold definition: a voltage can be applied obtaining the values for VIH and VIL.
OUT	5	MOSFET gate drive sourcing / sinking output controlled by the IN pin. A pull-down equivalent resistor [50 kΩ (typ.)] is present.

3 Maximum ratings

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (2-layer FR4 PCB, T_A = 27 °C natural convection)	250	°C/W
R_{thJC}	Thermal resistance junction to case	130	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-40 to 150	°C
T_A	Operating ambient temperature range	-40 to 125	°C

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit	Note
$V_{VCC,max}$	Maximum IC supply voltage	19	V	IN unconnected, IN_TH = 3.3 V
	Max. negative allowed voltage	- 0.3	V	
$V_{IN\_TH,max}$	Max. positive voltage at IN_TH pin	5.5	V	
	Max. negative allowed voltage	- 0.3	V	
$V_{IN,max}$	Maximum voltage at IN pin	5.5	V	
	Max. negative allowed voltage	- 0.3	V	
$I_{OUT,rms}$	Maximum RMS output current	100	mA	

4 Electrical characteristics

(V_{CC} = 12 V, V_{IN_TH} = 3.3 V, TJ = - 40 ÷ 125 °C, unless otherwise specified)

Table 5. Electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
IC SUPPLY							
V_{CC}	VCC	Operating range		10		18	V
$V_{CC,on}$	VCC	Turn-on threshold		9	10	11	V
$V_{UVLO,hyst}$	VCC	UVLO hysteresis		0.5	1		V
I_{ST-UP}	VCC	Start-up current	$V_{CC} = V_{CC,on}$ - 0.5 V			40	µA
$I_{CC,0}$	VCC	Static supply current	IN = 0 V			40	µA
$I_{CC,op}$	VCC	Operating supply current	See *Figure 4* and *Figure 5*				
IN_TH							
V_{IN_TH}	IN_TH	Operating range		2		5.5	V
$V_{IN\_TH,UV}$	IN_TH	IN_TH UVLO	IN_TH short with IN, rising edge		1.5		V
I_{IN_TH}	IN_TH	IN_TH pin bias current(1)				40	µA
INPUT							
V_{IH}/V_{IN_TH}	IN	Relative input high level threshold	(2)	36		58	%
V_{IL}/V_{IN_TH}	IN	Relative input low level threshold	(2)	25		46	%
V_{IN_Hyst}	IN	Hysteresis		7		25	%
IIN	IN	IN pin bias current	VIN = 5 V		50		µA
R_{INPD}	IN	Input pull-down resistance	$VIN = V_{IN\_TH}$		100		kΩ
T_{D_LH}	IN	IN to GD propagation delay	IN low to high, no load			30	ns
T_{D_HL}	IN	IN to GD propagation delay	IN high to low, no load			30	ns
OUTPUT							
$V_{OUT,H}$	OUT	OUT pin high level	Isrc = 100 mA, T_J = 25 °C		11.4		V
			Isrc = 100 mA, T_J = -40 ÷ 125 °C(1)		11.4		
$V_{OUT,L}$	OUT	OUT pin low level	Isnk = 100 mA, T_J = 25 °C		0.53		V
			Isnk = 100 mA, T_J = -40 ÷ 125 °C(1)		0.53		
I_{SRC}	OUT	Source current(1)	$V_{OUT} = V_{CC}$ / 2		940		mA
I_{SNK}	OUT	Sink current(1)	$V_{OUT} = V_{CC}$ / 2		1.1		A
t_R	OUT	Rise time	C_{OUT} = 470 pF			20	ns
t_F	OUT	Fall time	C_{OUT} = 470 pF			20	ns
R_{GPD}	OUT	Pull-down resistor			50		kΩ

1. Not tested in production.
2. Overlapping prevent by hysteresis V_{IN_Hyst}.

Figure 3. Timings

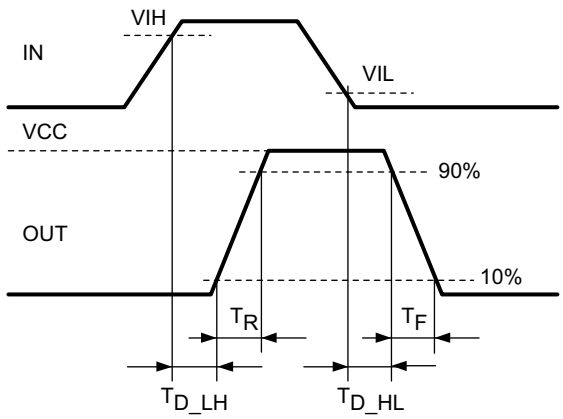


Figure 4. Operating supply current (no load)

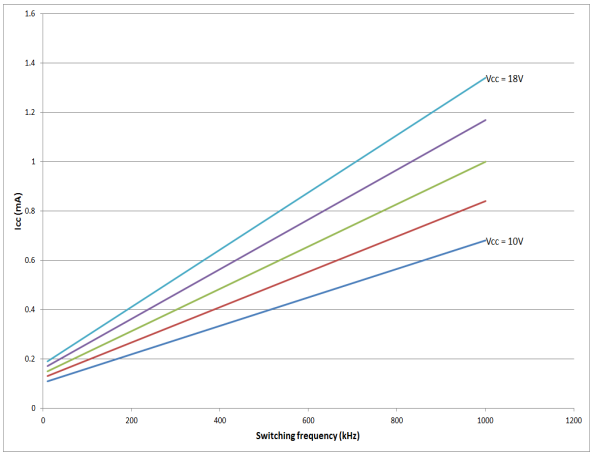


Figure 5. Operating supply current (C_{OUT} = 470 pF)

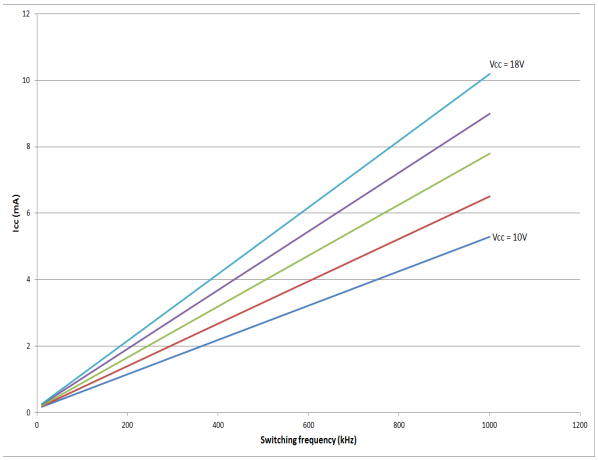
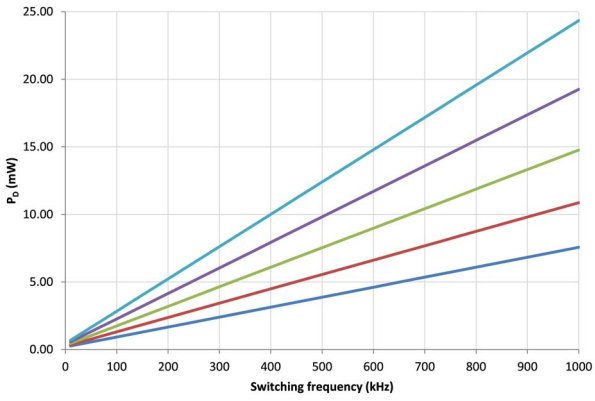


Figure 6. V_{CC} power dissipation (PD) when no load is applied



5 Typical applications

Figure 7. Test circuit

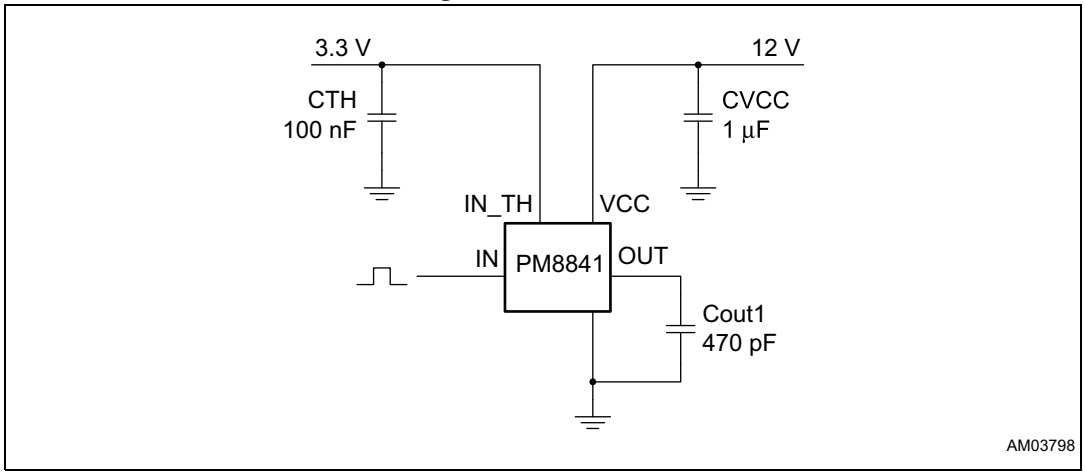


Figure 8. Digitally controlled PFC boost converter

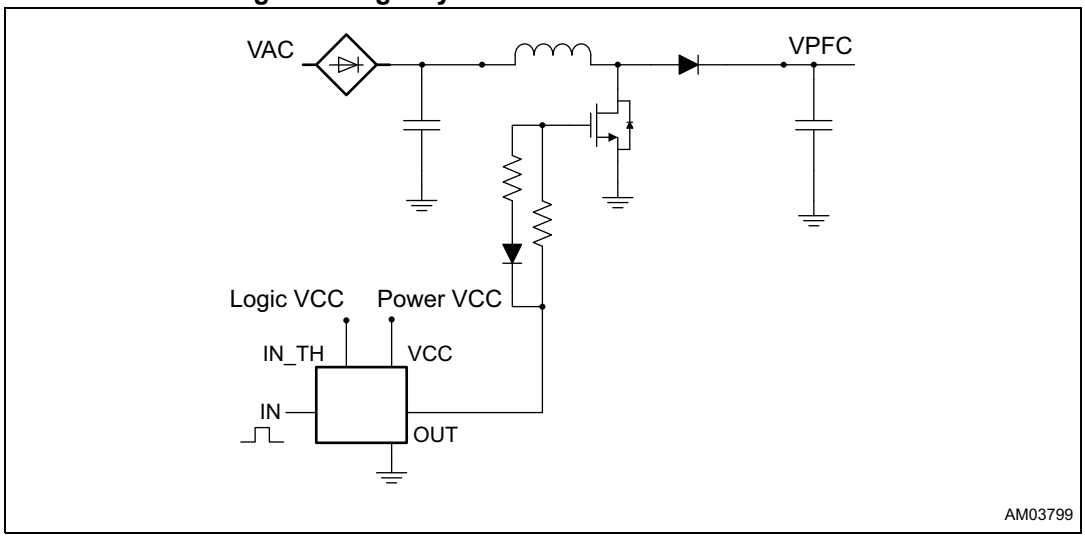


Figure 9. Digitally controlled flyback converter

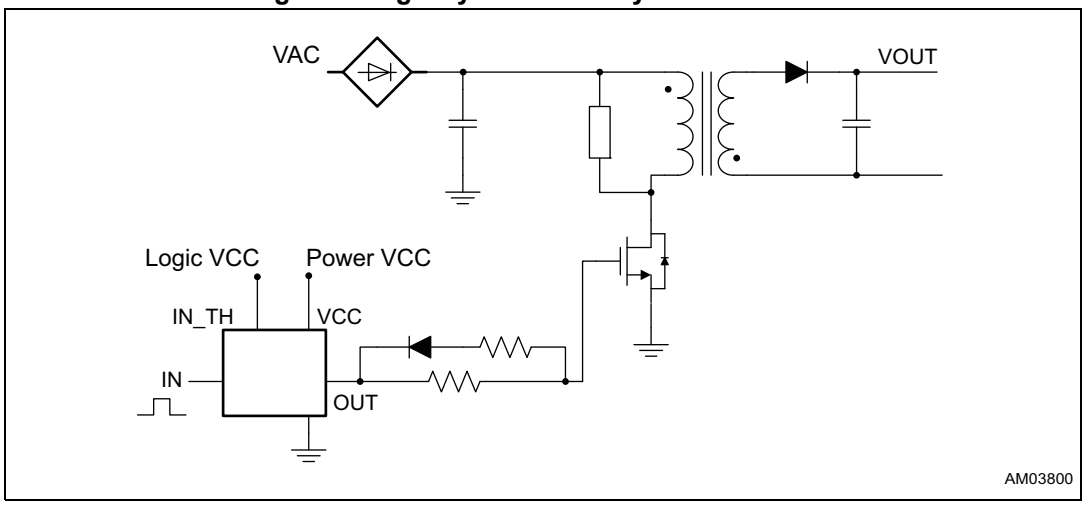
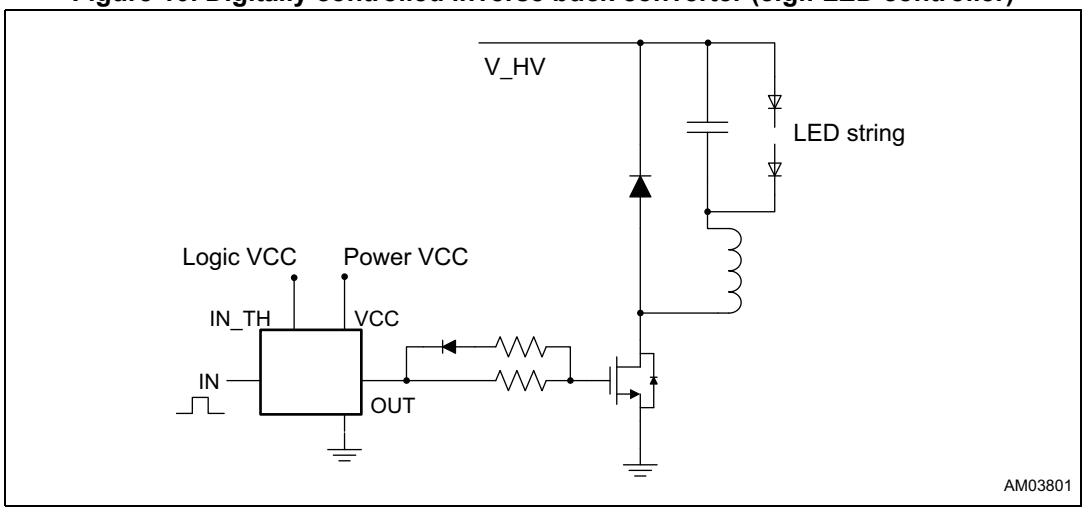


Figure 10. Digitally controlled inverse buck converter (e.g.: LED controller)



6 Application guidelines

6.1 Power supply

The PM8841 driver is intended to drive power MOSFETs used in power conversion topologies at high speed. The accurate supply voltage definition guarantees an effective driving in every condition. The voltage present at the IN_TH pin is used for the threshold definition. It could be the same voltage used to supply the device providing the signal applied to the IN pin, or it can be derived by the VCC pin, eventually using a voltage divider. It is mainly suggested to provide IN_TH voltage starting from VCC voltage.

For example, in *Figure 11*, an auxiliary, unregulated, voltage can be used to be connected to both PM8841 VCC pin and the input of a linear regulator that provides a well regulated supply voltage for logic circuitry. The same low voltage is then provided to the IN_TH pin of the PM8841.

If the IN_TH is derived directly by VCC pin, the structure illustrated in *Figure 12* can be used.

Figure 11. Shared supply configuration

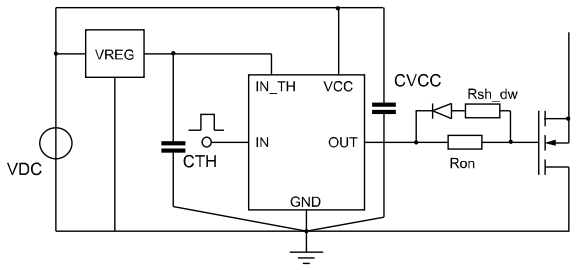
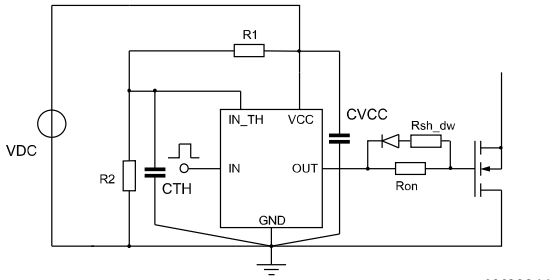


Figure 12. Independent supply configuration



It is mandatory to properly connect a 100 nF ceramic cap as close as possible to the VCC pin to bypass the current's spikes absorbed by VCC during the gate charging.

Also IN_TH voltage should be filtered with a ceramic capacitor (10 nF to 100 nF), especially when long traces are used to supply it; when derived by VCC a lighter filtering is allowed.

6.2 Layout suggestions

The small package of the PM8841 allows to place it very close to the gate of the driven MOSFET: this reduces the risk of injecting high frequency noise produced by the driving current running between the OUT pin and the MOSFET's gate pin.

6.3 Driving switches

The IN pin truth table is reported in *Table 6*.

Table 6. PM8841 truth table

IN	PM8841
High	High
Low	Low

Differential MOSFET's driving strength is seldom necessary in topologies such as flybacks or boost controlled in the peak current mode. A lower driving current is used to turn on the MOSFET in order to reduce the EMI produced by the Miller capacitance activation, while a stronger turn-off action is suggested to minimize the turn-off delay and, consequently the deviation between theoretical and practical behaviors.

The same asymmetrical driving strength is required when the IGBT switch is used: in fact the driving strength control is mandatory to avoid latch-up phenomena intrinsically related with this kind of the switch. The asymmetrical driving can be realized using a diode and resistance as illustrated in typical application diagrams (refer to the PM8851 device when accurate control of the asymmetrical driving current is required).

When low switching frequencies are required and propagation delays can be compensated, it is possible to drive contemporary the IN pin and the IN_TH pin to exploit the relevant UVLO threshold of the device (typ. 1.5 V) using the PM8841 as a fixed threshold device without any external component: care has to be taken to consider an additional propagation delay (typ. 300 ns) after the falling edge of the input signal.

6.4 Power dissipation

Overall power dissipation can be evaluated considering two main contributions: the device related consumption (PD) and the gate driving power demand (PG):

Equation 1

$$P_{Tot} = P_D + P_G$$

The device power consumption can be found in *Figure 6 on page 6*: it represents the power required by the device to supply internal structures and pull-downs resistors.

The gate driving power dissipation is the power required to deliver to and from the MOSFET's gate the required gate charge:

Equation 2

$$P_G = Q_g \times V_{gs} \times f_{sw}$$

The Q_g value can be found depicted into the MOSFET's datasheet for any applied V_{gs}: V_{gs} can considered equal to VCC.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 13. SOT23-5 package outline

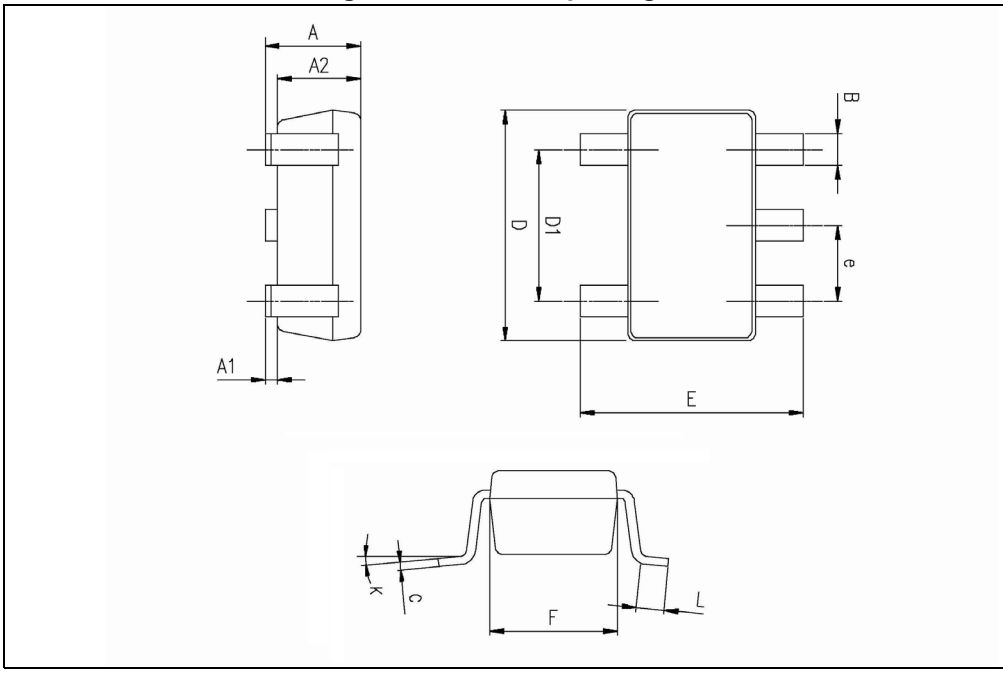


Table 7. SOT23-5 package mechanical data

Symbol	Dimensions (mm)			Dimensions (inches)			Note
	Typ.	Min.	Max.	Typ.	Min.	Max.	
A		0.90	1.45		0.035	0.057	
A1		0.00	0.15		0.000	0.006	
A2		0.90	1.30		0.035	0.051	
b		0.30	0.50		0.012	0.020	
c		0.09	0.20		0.004	0.008	
D		2.80	3.05		0.11	0.12	
E		1.50	1.75		0.059	0.069	
e	0.95			0.037			
H		2.60	3.00		0.102	0.118	
L		0.30	0.60		0.012	0.024	
q		0	10		0	10	Degrees

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
29-Oct-2014	1	Initial release.